

JEDEC STANDARD

**Wide I/O Single Data Rate
(Wide I/O SDR)**

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WIDE I/O SINGLE DATA RATE (WIDE I/O SDR)

(From JEDEC Board Ballot JCB-11-79, formulated under the cognizance of the JC-42.6 Subcommittee on Low Power Memories.)

1 Scope

This standard defines the Wide I/O specification, including features, functionality, AC and DC characteristics, packages, and micropillar signal assignments. This standard covers the following technologies: Wide I/O. The purpose of this standard is to define the minimum set of requirements for JEDEC compliant, 1 Gb through 32 Gb SDRAM (monolithic density) devices with 4, 128b wide channels using direct chip-to-chip attach methods between 1 to 4 memory devices and a controller device. This standard was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), LPDDR (JESD209), and LPDDR2 (JESD209-2). Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the Wide I/O standard.

2 General Description

2.1 Terms and Definitions

Within the Wide I/O standard, these terms have particular meanings:

Stack: All memory chips in the memory system taken together in one assembly.

NOTE This Wide I/O standard supports memory stacks that include up to 4 memory chips.

Slice: One memory chip in the stack of memory chips.

Rank: That portion of memory from one memory die that is logically connected to a single channel within the memory stack.

Channel: Both a set of physically discrete connections within the Wide I/O interface and a logically discrete, independently controlled partition of the Wide I/O interface.

NOTE The Wide I/O interface supports 4 physical and 4 logical channels. Each physical channel contains all the control, data and clock signals necessary to independently control each of the 4 logical channels in the Wide I/O interface. Aside from a few global configuration options, each logical channel has its own set of mode registers, can have different DRAM pages open, can be independently clocked and can even be in different power states. The physical channel also contains power and ground signals but all power and ground signals on all physical channels must be at their appropriate levels for any portion of the Wide I/O device to operate correctly. The physical channel also contains a reset signal but the Wide I/O interface defines reset to be per slice rather than per channel.

2.2 Micropillar-out

2.2.1 Key Features

- 128 Data Bits per channel
- Support for up to 32 Gbit monolithic density
- micropillars allocated for differential CK/DQS for future DDR extension
- 5 Serial Scan connections/channel + 1 overall serial enable
- Per byte write masks
- 1 “must be routed through substrate” Direct Access micropillar per channel
- 2 missing row vertical channel spacing, 6 missing column horizontal channel spacing
- Power micropillar count supports current requirements of low-power memory space

2.2.2 Micropillar Definitions

Table 1 — Micropillar Definitions

Micropillar Type	Count	Description
VDD1	6	Core Power
VDD2	20	Core Power
VDDQ	16	I/O Power
VSS	24	Core Ground
VSSQ	16	I/O Ground
DQ	128	Data
DQS	16	Data Strobe DQS_t, DQS_c (unused in current definition)
DM	16	Data Mask
ADDR	19	Address (0-16), Bank (0-1)
CMD	4	RAS_n, CAS_n, WE_n, RESET
CK	2	CK_t, CK_c (unused in current definition)
CS	4	Chip (Rank) Select
CKE	4	Clock Enable
TEST	1/0	Memory DA Test Mode Enable (only on channel A, location is DA(o) on other channels)
SER	5	Serial Boundary Scan micropillars (uses CS to select rank)
KEY	1	Vendor Specific micropillar in channel A, n/c in channel B, Scan Enable in channel C, missing micropillar in channel D.
NC	9	no connect
DA	1	Direct Access (all SoC vendors will provide direct connection to memory through substrate)
DA(o)	8/9	Direct Access (optional, SoC vendors may or may not provide direct connections to memory through substrate)
Total	300	

NOTE 1 All views are the bottom views looking down upon the memory micropillars, i.e., with the memory micropillars facing out of the page. In the anticipated mounting orientation, this will be looking up from the board.

NOTE 2 There are 10 NC micropillars in channel B and 9 NC micropillars in channel A, C and D. The NC micropillar will be with micro bump and the missing micropillar will be without micropillar and microbump.

2.2.3 Left Side of Array Showing Two of Four Channels

			Channel A							
			1	2	3	4	5	6	7	8
			C1	C2	C3	C4	C5	C6	C7	C8
			0	50	100	150	200	250	300	350
M	CA	520	VSS	A0a	VDD2	DA(o)7a	VSS	CK_ta	VDD2	TESTa
L	CB	480	VSS	A1a	VDD2	NC	VSS	CK_ca	VDD2	SDOa
K	CC	440	VPIN	A2a	A9a	A10a	BA1a	RAS_na	CS0_na	CS3_na
J	CD	400	VDD1	A3a	A8a	A11a	BA0a	CAS_na	CS1_na	CS2_na
H	CE	360	VDD1	A4a	A7a	A12a	A15a	WE_na	CKE0a	CKE3a
G	CF	320	VDD1	A5a	A6a	A13a	A14a	A16a	CKE1a	CKE2a
			nb	nb	nb	nb	nb	nb	nb	nb
			nb	nb	nb	nb	nb	nb	nb	nb
F	CF	200	VDD1	A5d	A6d	A13d	A14d	A16d	CKE1d	CKE2d
E	CE	160	VDD1	A4d	A7d	A12d	A15d	WE_nd	CKE0d	CKE3d
D	CD	120	VDD1	A3d	A8d	A11d	BA0d	CAS_nd	CS1_nd	CS2_nd
C	CC	80	KEY	A2d	A9d	A10d	BA1d	RAS_nd	CS0_nd	CS3_nd
B	CB	40	VSS	A1d	VDD2	NC	VSS	CK_cd	VDD2	SDOd
A	CA	0	VSS	A0d	VDD2	DA(o)7d	VSS	CK_td	VDD2	DA(o)8d
			0	50	100	150	200	250	300	350
			C1	C2	C3	C4	C5	C6	C7	C8
			1	2	3	4	5	6	7	8
			Channel D							

Figure 1 — Left Side of Array Showing Two of Four Channels

2.2.4 Channel A Micropillar Locations

			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15
			0	50	100	150	200	250	300	350	400	450	500	550	600	650	700
M	CA	520	VSS	A0a	VDD2	DA(o)7a	VSS	CK_ta	VDD2	TESTa	VSS	VSS	DM0a	DA(o)6a	DM1a	VDD2	VDD2
L	CB	480	VSS	A1a	VDD2	NC	VSS	CK_ca	VDD2	SD0a	VSS	VSS	D06a	NC	D011a	VDD2	VDD2
K	CC	440	VPIN	A2a	A9a	A10a	BA1a	RAS_na	CS0_na	CS3_na	SCk6a	DQ0a	VSSQ	DQ00_ca	VDDQ	DQ12a	DQ28a
J	CD	400	VDD1	A3a	A8a	A11a	BA0a	CAS_na	CS1_na	CS2_na	SD1a	DQ1a	VSSQ	DQ00_ta	VDDQ	DQ13a	DQ29a
H	CE	360	VDD1	A4a	A7a	A12a	A15a	WE_na	CKE0a	CKE3a	SSH_na	DQ2a	DQ6a	DQ7a	DQ10a	DQ14a	DQ30a
G	CF	320	VDD1	A5a	A6a	A13a	A14a	A16a	CKE1a	CKE2a	SOE_na	DQ3a	DQ4a	DQ8a	DQ9a	DQ15a	DQ31a
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
C16	C17	C18	C19	C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	C32	
750	800	850	900	950	1000	1050	1100	1150	1200	1250	1300	1350	1400	1450	1500	1550	
DM3a	DA(o)5a	DM2a	VSS	VSS	DM4a	DA(o)4a	DM5a	VDD2	VDD2	DM7	DA(o)3a	DM6a	VSS	VSS	DM8a	DA(o)2a	
DQ27a	NC	DQ22a	VSS	VSS	DQ38a	NC	DQ43a	VDD2	VDD2	DQ69a	NC	DQ64a	VSS	VSS	DQ70a	NC	
VDDQ	DQS1_ca	VSSQ	DQ16a	DQ32a	VSSQ	DQS2_ca	VDDQ	DQ44a	DQ60a	VDDQ	DQS3_ca	VSSQ	DQ48a	DQ64a	VSSQ	DQS4_ca	
VDDQ	DQS1_ta	VSSQ	DQ17a	DQ33a	VSSQ	DQS2_ta	VDDQ	DQ45a	DQ61a	VDDQ	DQS3_ta	VSSQ	DQ49a	DQ65a	VSSQ	DQS4_ta	
DQ26a	DQ23a	DQ21a	DQ18a	DQ34a	DQ37a	DQ39a	DQ42a	DQ46a	DQ62a	DQ68a	DQ65a	DQ63a	DQ65a	DQ66a	DQ68a	DQ71a	
DQ25a	DQ24a	DQ20a	DQ19a	DQ35a	DQ36a	DQ40a	DQ41a	DQ47a	DQ63a	DQ67a	DQ66a	DQ62a	DQ65a	DQ67a	DQ68a	DQ72a	
33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
C33	C34	C35	C36	C37	C38	C39	C40	C41	C42	C43	C44	C45	C46	C47	C48	C49	C50
1600	1650	1700	1750	1800	1850	1900	1950	2000	2050	2100	2150	2200	2250	2300	2350	2400	2450
DM9a	VDD2	VDD2	DM11a	DA(o)1a	DM10a	VSS	VSS	DM12a	DA(o)0a	DM13a	VDD2	VDD2	DM15a	DAa	DM14a	VSS	VSS
Q75a	VDD2	VDD2	DQ91a	NC	DQ86a	VSS	VSS	DQ102a	NC	DQ107a	VDD2	VDD2	DQ123a	NC	DQ118a	VSS	VSS
VDDQ	DQ76a	DQ92a	VDDQ	DQS5_c	VSSQ	DQ80a	DQ96a	VSSQ	DQS6_ca	VDDQ	DQ108a	DQ124a	VDDQ	DQS7_ca	VSSQ	DQ112a	VSS
VDDQ	DQ77a	DQ93a	VDDQ	DQS5_ta	VSSQ	DQ81a	DQ97a	VSSQ	DQS6_ta	VDDQ	DQ109a	DQ125a	VDDQ	DQS7_ta	VSSQ	DQ113a	VSS
Q74a	DQ78a	DQ94a	DQ90a	DQ87a	DQ86a	DQ82a	DQ98a	DQ101a	DQ103a	DQ106a	DQ110a	DQ126a	DQ122a	DQ119a	DQ117a	DQ114a	VDD
Q73a	DQ79a	DQ95a	DQ89a	DQ88a	DQ84a	DQ83a	DQ99a	DQ100a	DQ104a	DQ105a	DQ111a	DQ127a	DQ121a	DQ120a	DQ116a	DQ115a	RST0

Figure 2 — Channel A Micropillar Locations

2.2.5 Center Area of 4-Channel Map

Channel A										Channel B									
14	45	46	47	48	49	50				51	52	53	54	55	56	57			
44	C45	C46	C47	C48	C49	C50				C50	C49	C48	C47	C46	C45	C44			
150	2200	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700	2750	2800	2850	2900	2950			
D02	VDD2	DM15a	D4a	DM14a	VSS	VSS	nb	nb	nb	VSS	VSS	DM14b	D4b	DM15b	VDD2	VDD2			
D02	VDD2	DQ123a	NC	DQ118a	VSS	VSS	nb	nb	nb	VSS	VSS	DQ118b	NC	DQ123b	VDD2	VDD2			
r108a	DQ124a	VDDQ	DCS7_ca	VSSQ	DQ112a	VDD1	nb	nb	nb	VDD1	DQ112b	VSSQ	DCS7_db	VDDQ	DQ124b	DQ124b			
r108a	DQ125a	VDDQ	DCS7_b	VSSQ	DQ113a	VDD1	nb	nb	nb	VDD1	DQ113b	VSSQ	DCS7_b	VDDQ	DQ125b	DQ125b			
r110a	DQ126a	DQ122a	DQ119a	DQ117a	DQ114a	VDD1	nb	nb	nb	VDD1	DQ114b	DQ117b	DQ119b	DQ122b	DQ126b	DQ126b			
r111a	DQ127a	DQ121a	DQ120a	DQ116a	DQ115a	RST0_n	nb	nb	nb	RST1_n	DQ115b	DQ116b	DQ120b	DQ121b	DQ127b	DQ127b			
nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb			
nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb	nb			
r111d	DQ127d	DQ121d	DQ120d	DQ116d	DQ115d	RST3_n	nb	nb	nb	RST2_n	DQ115c	DQ116c	DQ120c	DQ121c	DQ127c	DQ127c			
r110d	DQ126d	DQ122d	DQ119d	DQ117d	DQ114d	VDD1	nb	nb	nb	VDD1	DQ114c	DQ117c	DQ119c	DQ122c	DQ126c	DQ126c			
r109d	DQ125d	VDDQ	DCS7_b	VSSQ	DQ113d	VDD1	nb	nb	nb	VDD1	DQ113c	VSSQ	DCS7_b	VDDQ	DQ125c	DQ125c			
r108d	DQ124d	VDDQ	DCS7_a	VSSQ	DQ112d	VDD1	nb	nb	nb	VDD1	DQ112c	VSSQ	DCS7_a	VDDQ	DQ124c	DQ124c			
D02	VDD2	DQ123d	NC	DQ118d	VSS	VSS	nb	nb	nb	VSS	VSS	DQ118c	NC	DQ123c	VDD2	VDD2			
D02	VDD2	DM15d	D4d	DM14d	VSS	VSS	nb	nb	nb	VSS	VSS	DM14c	D4c	DM15c	VDD2	VDD2			
150	2200	2250	2300	2350	2400	2450	2500	2550	2600	2650	2700	2750	2800	2850	2900	2950			
44	C45	C46	C47	C48	C49	C50				C50	C49	C48	C47	C46	C45	C44			
14	45	46	47	48	49	50				51	52	53	54	55	56	57			
Channel D										Channel C									

Figure 3 — Center Area of 4-Channel Map

Note the channel spacing and the micropillar assignments are reflections of Channel A.

The overall array size is (5.25mm + 1 micropillar diameter) x (0.52mm + 1 micropillar diameter).

The pitch (center to center) is 40 microns in the vertical dimension and 50 microns in the horizontal dimension.

2.3 Input/Output Functional Description

2.3.1 Micropillar Definition and Description

Note on nomenclature: unless otherwise designated, each channel is independent and implements independent sets of the designated micropillars. The channels are designated “a” to “d”. Additionally, unless otherwise designated, all signals are directly connected to all ranks (0 to 3) in the stack.

Table 2 — Micropillar Definition and Description

Name	Type	Description
CK_t[a:d]	Input	Clock: CK_t is a single-ended clock input. All Control, Address and Write Data (DQ) inputs are sampled on the positive edge of CK_t. The positive clock edge is defined by CK_t crossing 50% VDDQ.
CKE[0:3][a:d]	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. Each of CKE[0:3][a:d] address a single rank (0 to 3) on each of the channels (a to d).
CS[0:3]_n[a:d]	Input	Chip Select: CS_n is considered part of the command code. See Command Truth Table for command code descriptions. Each of CS[0:3]_n[a:d] address a single rank (0 to 3) on each of the channels (a to d).
RAS_n[a:d], CAS_n[a:d], WE_n[a:d]	Input	Command Inputs: Uni-directional command inputs. RAS_n, CAS_n and WE_n define the command being selected. See Command Truth Table for command code descriptions.
A[0:16][a:d]	Input	Address Inputs: Uni-directional address inputs. These provide the Row Address inputs for activate commands, the Column Address and Auto Precharge inputs for Read and Write commands, the Short Preamble inputs for Read commands, and the opcode for the Mode Register Set commands.
A10/AP[a:d]	Input	Autoprecharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (High: Autoprecharge, Low: No Autoprecharge)
A11/SP[a:d]	Input	Short Preamble: The controller indicate read with short preamble by driving A11 high when signalling a read command.
BA[0:1][a:d]	Input	Bank Inputs: Uni-directional bank select inputs. These provide the Bank Select inputs for activate, read, write and precharge commands.
RST[0:3]_n	Input	Reset Input: Uni-directional reset input. Each reset line resets all channels in a single slice. RST[0]_n appears on channel a and resets slice 0 (corresponding to CKE0/CS0_n) RST[1]_n appears on channel b and resets slice 1, RST[2]_n appears on channel c and resets slice 2, RST[3]_n appears on channel d and resets slice 3.
DQ[0:127] [a:d]	I/O	Data Inputs/Output: Bi-directional data bus
DQS[0:7]_t [a:d]	Output (possibly I/O in future)	Data Strobe: Data strobe (DQS_t) is output only in the current definition. Memories generate DQS_t such that a positive or a negative edge of DQS_t occurs in the middle of the read data eye with DQ providing a setup and a hold time to the DQS edge. Each DQS_t strobes two bytes of data. For timing purposes, the DQS edge is defined by DQS_t crossing 50% VDDQ. Note: write data is sampled on the positive edge of CK_t. In future extensions, DQS_t may be bidirectional.
DM[0:15][a:d]	Input	Input Data Mask: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on the rising edge of CK_t coincident with the write data. Although DM is for input only, the DM loading shall match DQ, DQS_t and DQS_c. DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-DQ15, and so on, i.e., DM15 is the input data mask signal for data on DQ120-DQ127.
TEST	Input	Test: This input makes memory DA test mode enable. It may be routed through a controller I/O buffer before driving the memory I/O pad. Its function is defined by each individual memory vendor.
SDI[a:d], SCK[a:d], SOE_n[a:d], SSH_n[a:d]	Input	Boundary Scan Inputs: These inputs provide the necessary connections for the memory boundary scan functionality as defined in Section 5.

Name	Type	Description
SDO[a:d]	Output	Boundary Scan Outputs: This output provides the necessary connection for the memory boundary scan functionality as defined in Section 5.
DA[a:d]	Input/O utput	Direct Access Input/Output: This I/O is used by memory for direct access test functionality. It must be routed directly to an external package I/O pad. Its function is defined by each individual memory vendor.
DA(o)[0:7] [a:d] DA(o)8[b:d]	Input/O utput	Direct Access Input/Output: This I/O is used by memory for direct access test functionality. It may be routed through a controller I/O buffer before driving an external package I/O pad. Their functions are defined by each individual memory vendor.
KEY		This is a missing micropillar in the array used to indicate array orientation. It appears only in channel D.
VPIN	Input	This micropillar is used to select vendor specific features. It appears only in channel A.
SSEN	Input	This micropillar is used to set the entire DRAM to boundary scan mode (high) or normal operation mode (low). It appears only on channel C.
CK_c[a:d]		This is the compliment of CK_t. It is not currently used by the Wide I/O standard. It is included only for future extension.
DQS[0:7]_c [a:d]		These are the compliments of DQS_t. They are not currently used by the Wide I/O standard. They are included only for future extension.
NC		No connect pads.
V _{DD1}	Supply	Core Power Supply 1: Core power supply.
V _{DD2}	Supply	Core Power Supply 2: Core and input buffer power supply.
V _{DDQ}	Supply	I/O Power Supply: Power supply for Data input/output buffers.
V _{SS}	Supply	Ground
V _{SSQ}	Supply	I/O Ground

2.4 Addressing

Wide I/O has 4 channels and total x512 bit I/Os. Each channel has 4 Banks and x128 bit I/Os.

Table 3 — Wide I/O Addressing

Device Density	Density / Channel	Address		
		BA	Row	Column
1Gb	256Mb	BA0 - BA1	RA0 - RA11	CA0 - CA6
2Gb	512Mb	BA0 - BA1	RA0 - RA12	CA0 - CA6
4Gb	1Gb	BA0 - BA1	RA0 - RA13	CA0 - CA6
8Gb	2Gb	BA0 - BA1	RA0 - RA14	CA0 - CA6
16Gb	4Gb	BA0 - BA1	RA0 - RA14	CA0 - CA7
32Gb	8Gb	TBD	TBD	TBD

3 Functional Description

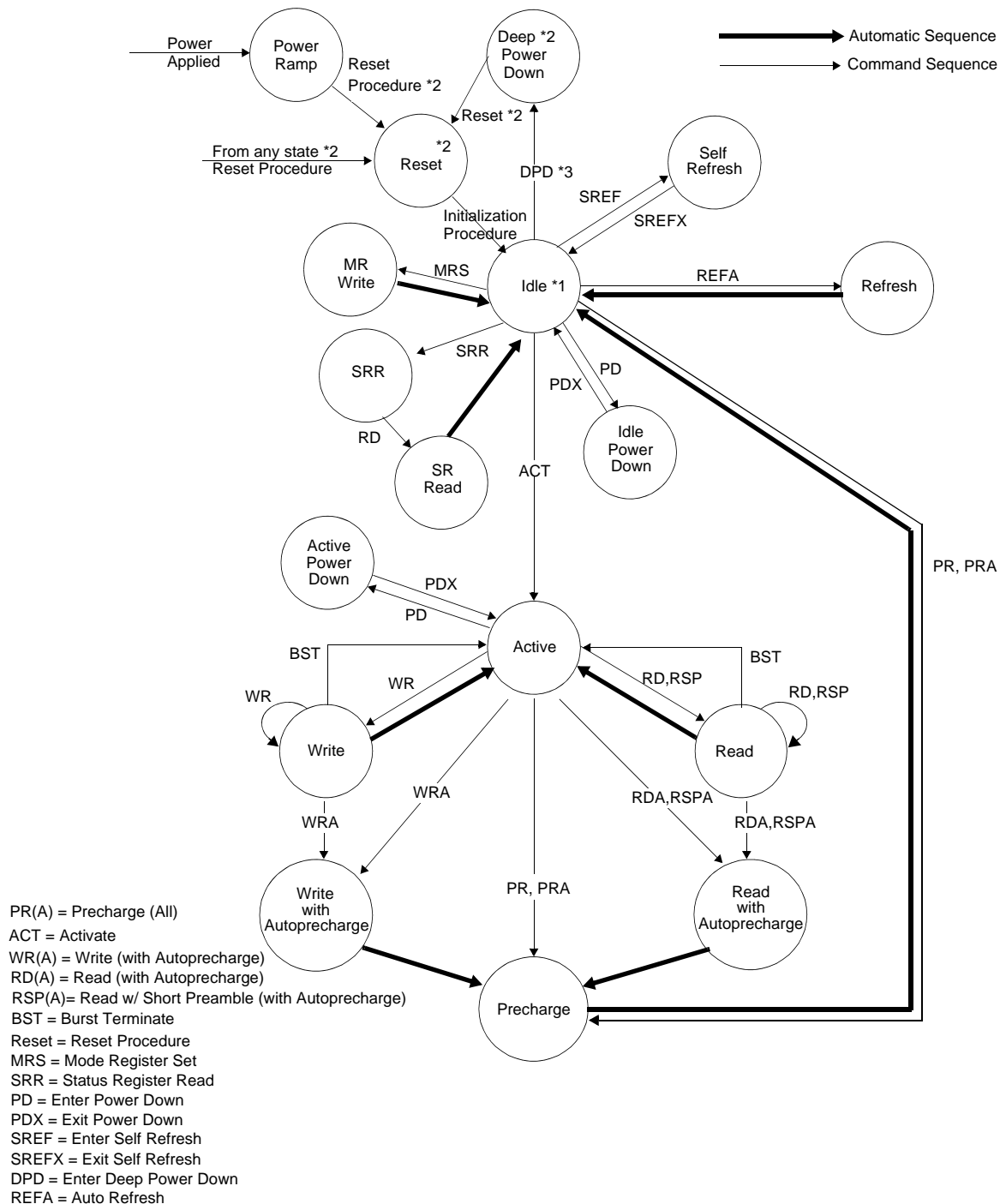
3.1 Wide I/O State Diagram

Wide I/O DRAM device state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. Unless otherwise specified, the state diagram describes the state and commands for only one channel in a slice.

For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

3.1 Wide I/O State Diagram (cont'd)

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restriction when considering the actual state of the banks.



NOTE 1 For Wide I/O DRAM in the Idle state, all banks are precharged.

NOTE 2 Reset Function are per slice (not per channel)

NOTE 3 After all channels in a slice receives the DPD command, the internal power circuit will enter off state IDD8.

Figure 4 — Wide I/O DRAM: Simplified State Diagram

3.2 Power up, Initialization and Power Off Sequence

3.2.1 Power-up, Initialization, and Power-Off

Wide I/O DRAM Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence shall be used to power up the Wide I/O DRAM device. Unless specified otherwise, these steps are mandatory.

3.2.2 Power-up and Initialization Sequence

1. Power Ramp: While applying power, RST_n is recommended to be maintained below $0.2 \times VDD2$; all other inputs shall be between VIL_{min} and VIH_{max} . The following conditions apply:
 - T_a is the point where any power supply first reaches 300 mV.
 - T_b is the point when all supply voltages are within their respective min/max operating conditions.
 - After T_a is reached, $VDD1$ must be greater than $VDD2 - 200$ mV.
 - After T_a is reached, $VDD1$ and $VDD2$ must be greater than $VDDQ - 200$ mV.
 - The voltage difference between VSS and $VSSQ$ micropillars may not exceed 100 mV.
 - The above conditions apply between T_a and power-off (controlled or uncontrolled).
 - Power ramp duration t_{INIT0} ($T_b - T_a$) must be no greater than 20 ms and power ramp slope must be monotonic during t_{INIT0} .
 - The Wide I/O DRAM device will guarantee that outputs are in a high impedance state while RST_n is held low.
2. RST_n: RST_n must be maintained for a minimum 200 us with stable power. CKE must be pulled “Low” a minimum of 10ns before RST_n is de-asserted.
3. CKE and Clock: After RST_n is de-asserted, CKE must remain deasserted for 500 us. During this time, the DRAM will initialize internal state independent of external clocks.

The clock must be started and stable for at least 5 clocks before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (t_{IS}) must also be met. Also, a NOP or Deselect command must be registered (with t_{IS} set up time to clock) the clock before CKE goes active. After CKE is registered high, t_{INIT5} must pass before issuing the MRS command to load a mode register.
4. Mode Register: Issue MRS Command(s) to load mode registers with all application settings.
5. Normal Operation: The Wide I/O DRAM device is now ready for normal operation.

Table 4 — Timing Parameters for initialization

Symbol	Value		Unit	Comment
	Min	Max		
t_{INIT0}		20	ms	Maximum Power Ramp Time
t_{INIT1}	200		us	Minimum RST_n low Time with stable power
t_{INIT2}	10		ns	Minimum CKE low Time before RST_n high
t_{INIT3}	500		us	Minimum CKE low Time after RST_n high
t_{INIT4}	5		tCK	Minimum stable clock before first CKE high
t_{INIT5}	200		us	Minimum idle time after first CKE assertion

3.2.2 Power-up and Initialization Sequence (cont'd)

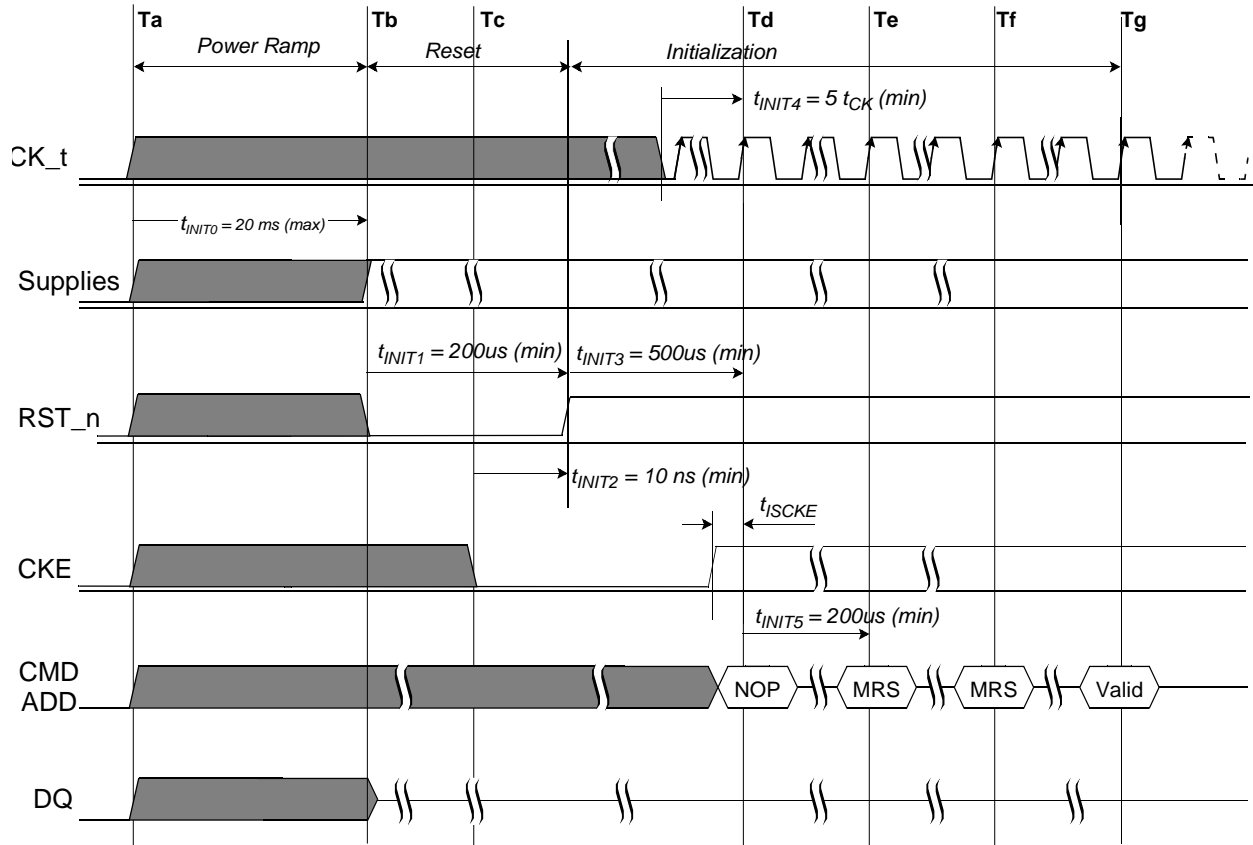


Figure 5 — Power Ramp and Initialization Sequence

3.2.3 Reset Initialization with Stable Power

The following sequence is required for RESET with no power interruption initialization.

1. Assert RST_n (active low) anytime when reset is needed. All other inputs may be undefined.
RST_n must be maintained for at least 100 ns. CKE must be pulled “LOW” 10ns before RST_n is deasserted.
2. Follow the Power-up and Initialization Sequence steps 3 and 4.
3. The Reset sequence is now completed; The Wide I/O DRAM device is ready for normal operation.

3.2.3 Reset Initialization with Stable Power (cont'd)

Table 5 — Timing Parameters for Reset Initialization with stable Power

Symbol	Value		Unit	Comment
	min	max		
t_{INIT1}	100		ns	Minimum RST_n low Time for Reset Initialization with stable power
t_{INIT2}	10		ns	Minimum CKE low Time before RST_n high
t_{INIT3}	500		us	Minimum CKE low Time after RST_n high
t_{INIT4}	5		tCK	Minimum stable clock before first CKE high
t_{INIT5}	200		us	Minimum idle time after first CKE assertion

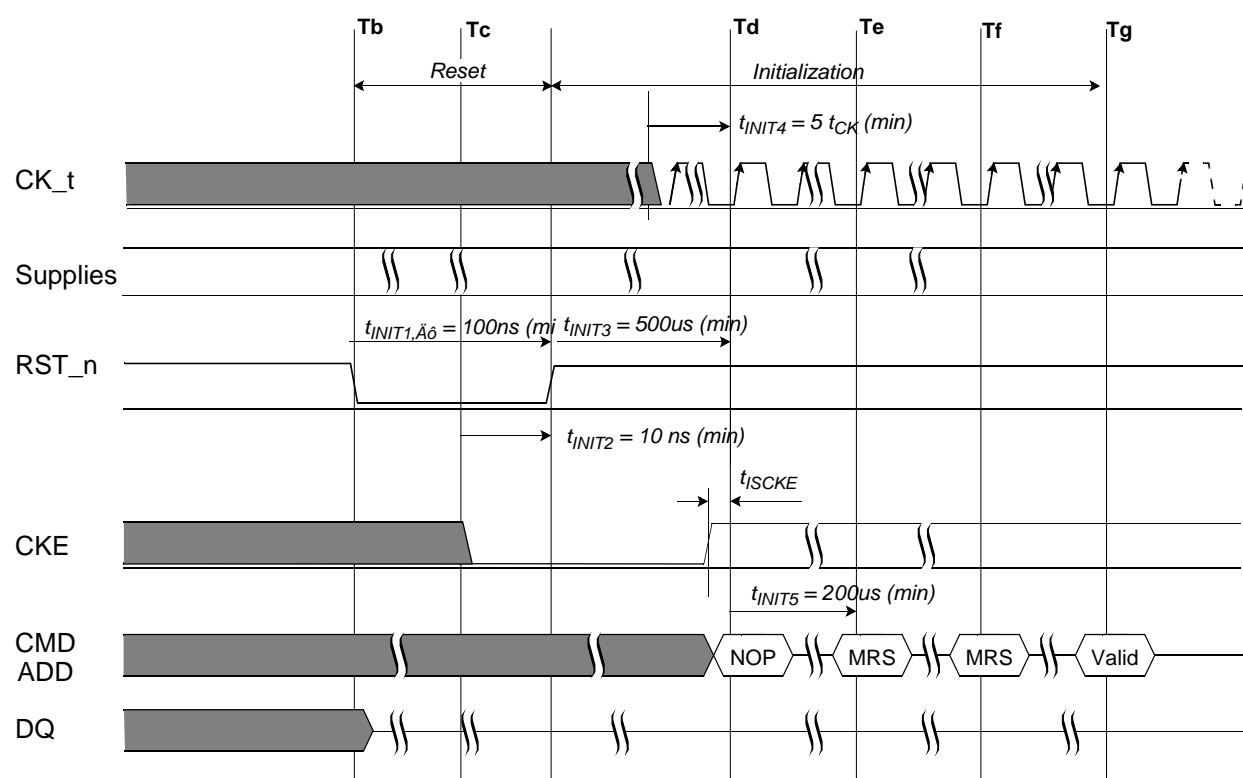


Figure 6 — Reset Initialization with stable Power

3.2.4 Power-off Sequence

The following sequence shall be used to power off the Wide I/O DRAM device. Unless specified otherwise, these steps are mandatory.

If system requires DQ remain Hi-Z while removing power, RST_n shall be held at a logic low level ($\leq 0.2 \times VDD2$) or CKE shall be held in logic low level. All other inputs shall be between VILmin and VIHmax. The Wide I/O DRAM device will guarantee that outputs are in a high impedance state while RST_n is held low.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.

The following conditions apply:

Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

The voltage difference between VSS and VSSQ micropillars may not exceed 100 mV.

Table 6 — Power-off Sequence

Symbol	Value		Unit	Comment
	min	max		
tPOFF	-	2	s	Maximum Power-Off ramp time

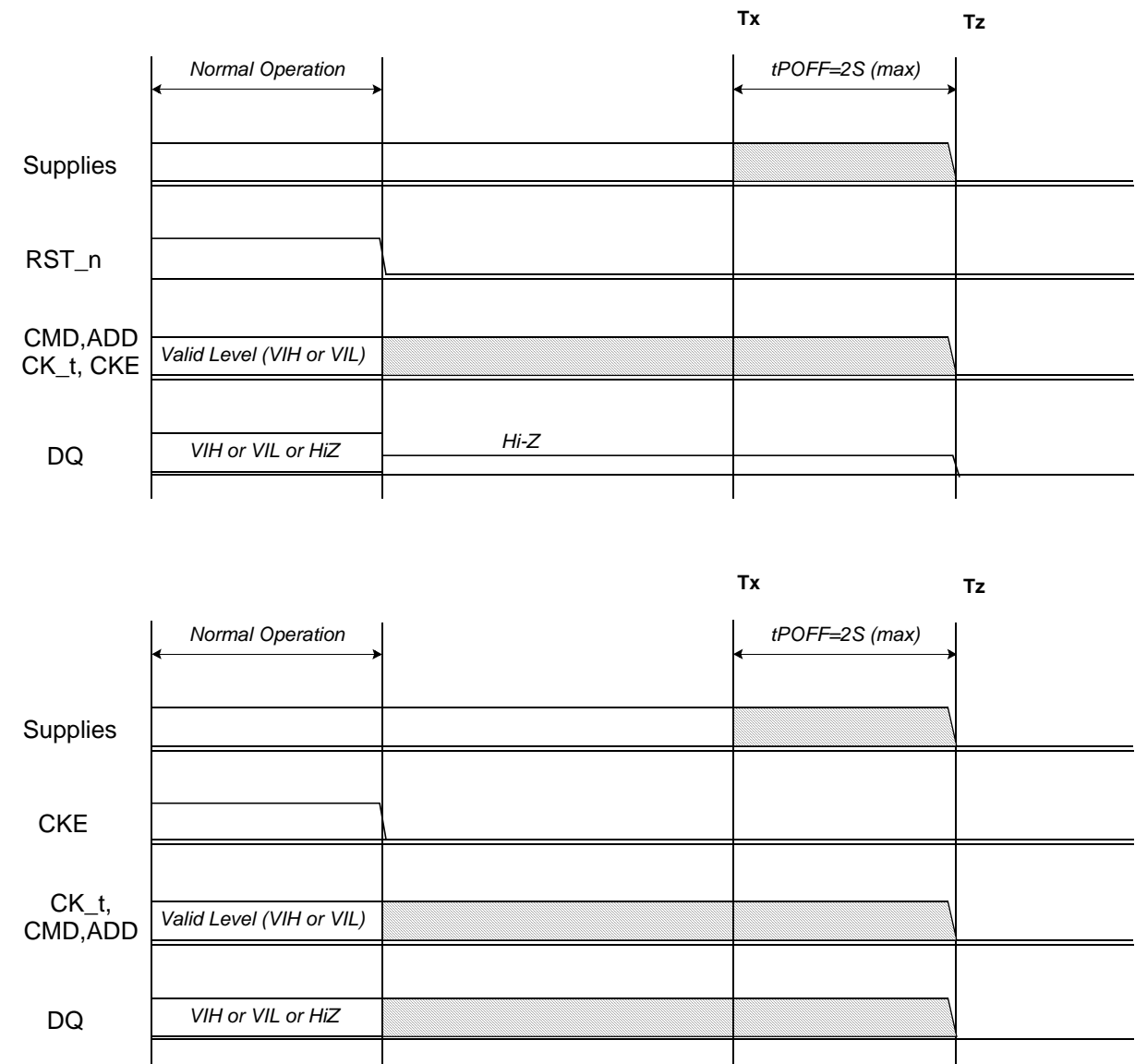


Figure 7 — Power-Off Sequence

3.2.5 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the Wide I/O device under uncontrolled condition. Unless specified otherwise, these steps are mandatory.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

T_z is the point where all power supplies first reaches 300 mV. After T_z, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/usec between Tx and Tz.

The uncontrolled power off sequence can be applied only up to 400 times in the life of the device

3.3 Mode Register Definition

3.3.1 Register Definition

For application flexibility, various functions, features, and modes are programmable in Wide I/O DRAM Mode Registers. Values are programmed into Mode Registers via a Mode Register Set (MRS) command. The default values of the Mode Registers (MR#) are not defined so they must be programmed during the reset and initialization sequence. The Mode Registers are defined for one channel.

The contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register will be redefined when the MRS command is issued.

MRS commands do not affect array contents regardless of when these commands are executed.

After the mode register set command, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.

The mode registers are divided into various fields depending on the functionality and/or modes.

Table 7 — Mode Register Definition

	A16	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MR0	0	0	0	0					Write Latency			TM	Read Latency			0	Burst Length		
MR1	0	0	1	Currently only one register is defined at A[15:0] = 0, DQ0-20 is used for SRR.															
MR2	0	1	0	0					nWR			TM	Drive Strength		0			Thermal Offset	
MR3	0	1	1	PASR															
MR4	1	0	0	Reserved for future use															
MR5	1	0	1	0								DQ/DQS Tuning							
MR6	1	1	0	Reserved for future use															
MR7	1	1	1	PASR															

3.3.2 Mode Register MR0

Mode register MR0 stores the data for controlling various operating modes of Wide I/O DRAM. It controls Burst Length, Read latency, and Write Latency.

A16	BA1	BA0	A15 - A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	Write Latency			TM	Read Latency			0	Burst Length		

A7	Mode
0	Normal
1	Test

A2	A1	A0	Burst length
0	0	0	Reserved
0	0	1	2
0	1	0	4
Others			Reserved

A10	A9	A8	Write Latency
0	0	1	WL=1
0	1	0	WL=2(Optional)
Others			Reserved

A6	A5	A4	Read Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	RL=2
0	1	1	RL=3
1	0	0	RL=4(Optional)
Others			Reserved

Figure 8 — Mode register MR0 definition

3.3.2.1 Burst Length

Read and write accesses to the Wide I/O DRAM are burst oriented, with the burst length being set as in Figure8 with the burst order as in Table 8.

The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2 or 4 locations are available for the sequential burst types.

Table 8 — Burst Length

Burst Length	Starting Column address		Order of accesses within a burst (Hexadecimal notation)
	A1	A0	Sequential
2		0	0-1
		1	1-0
4	0	0	0-1-2-3
	0	1	1-2-3-0
	1	0	2-3-0-1
	1	1	3-0-1-2

NOTE 1 For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.

NOTE 2 For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.

NOTE 3 Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to four

NOTE 4 (where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

3.3.2.2 Read Latency

The READ latency is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tAC delay for the first piece of output data is measured.

If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at $n + 3t_{CK} + t_{AC}$. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at $n + 2t_{CK} + t_{AC}$.

3.3.2.3 Write Latency

The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock where the first piece of input data is written.

If a WRITE command is registered at a clock edge n and the latency is 1 clock, the first data element will appear on the data bus at $n + t_{CK}$.

3.3.3 Mode Register MR1

The mode register MR1 is for SRR uses.

DQ127-DQ21	DQ20	DQ19	DQ18	DQ17	DQ16	DQ15	DQ14	DQ13	DQ12	DQ11-DQ10	DQ9	DQ8	DQ7-DQ4	DQ3	DQ2	DQ1	DQ0
Reserved	Temp. sensor location			Delay Step		Die Density			DT	Reserved	Refresh Interval		Reserved	Manufacturer ID			

DQ15	DQ14	DQ13	Die Density
0	0	0	1Gb
0	0	1	2Gb
0	1	0	4Gb
0	1	1	8Gb
1	0	0	16Gb
1	0	1	32Gb
1	1	0	Rsrv.
1	1	1	Rsrv.

DQ12	Device Type
0	Wide I/O SDR
1	Rsrv.

DQ9	DQ8	Refresh Interval
0	0	tREFI
0	1	0.50 x tREFI
1	0	0.25 x tREFI
1	1	High Temp. limit exceeded

DQ3	DQ2	DQ1	DQ0	Manufacturer's ID
0	0	0	0	Rsrv.
0	0	0	1	Samsung
0	0	1	0	Rsrv.
0	0	1	1	Elpida
0	1	0	0	Etron
0	1	0	1	Nanya
0	1	1	0	Hynix
0	1	1	1	Rsrv.
1	0	0	0	Winbond
1	0	0	1	ESMT
1	0	1	0	Rsrv.
1	0	1	1	Rsrv.
1	1	0	0	Rsrv.
1	1	0	1	Rsrv.
1	1	1	0	Rsrv.
1	1	1	1	Micron

DQ20	DQ19	DQ18	Temp. Sensor Location
0	0	0	Makes it reserved for Temp sensor location within a slice
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

DQ17	DQ16	Delay Step
0	0	No step
0	1	8 step
1	0	16 step
1	1	32 step

Figure 9 — Mode register MR1 definition

3.3.3.1 Status Register Read

SRR provides a method to read registers from the Wide I/O DRAM. The encoding for an SRR command is the same as a MRS with (A16, BA[1:0]) = “001”, MR1, status register. The address micropillars (A[15:0]) encode which register is to

be read. Currently only one register is defined at A[15:0] = 0. Refer to Table 1 for the definition of this register. The sequence to perform an SRR command is as follows:

all reads/writes must be completed

all banks must be closed

issue MRS with (A16, BA[1:0]) = 001 (SRR)

wait tSRR

issue read to any bank with A[15:0] = 0

Read latency cycles later the Wide I/O DRAM returns the status register data as it would a normal read

tSRC after the Read command, the Wide I/O DRAM will return to Idle (all banks precharged) state.

Refer to Figure 10 for Status register read sequence.

The burst length for the SRR read is always fixed to length 2.

The 1st bit of data and the 2nd bit of data on each DQ are the same. (DQn=DQn+1)

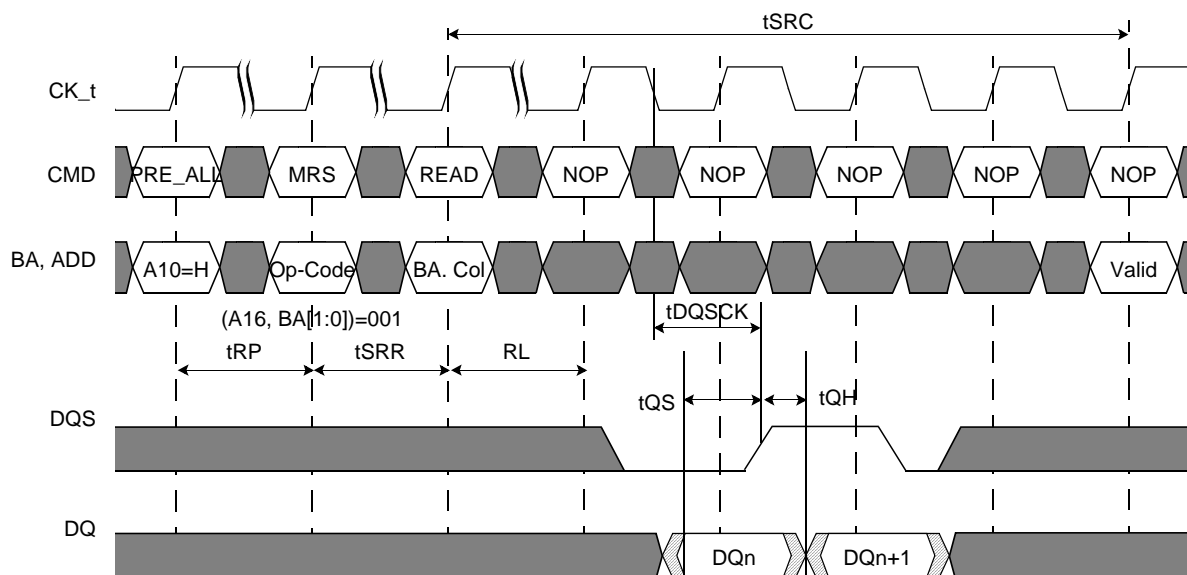


Figure 10 — Status Register Read Timing Diagram

NOTE1 SRR can only be issued after power-up and initialization sequence is complete;

NOTE2 SRR can only be issued with all banks precharged;

NOTE3 SRR RL is unchanged from value in the mode register;

NOTE4 SRR BL is fixed at 2. DQ_n and DQ_{n+1} values are the same.

3.3.4 Mode Register MR2

Mode register MR2 stores the data for controlling various operating modes of Wide I/O DRAM. It controls Thermal Offset, Drive Strength, TM and nWR.

A16	BA1	BA0	A15 -A10	A9	A8	A7	A6	A5	A4 - A1	A0
0	1	0	0	nWR		TM	Drive Strength		0	Thermal Offset

A7	Mode	A0	Thermal Offset
0	Normal	0	<5
1	Test	1	5-15

A9	A8	nWR
0	0	Reserved (2)
0	1	nWR=3
1	0	Reserved (4)
1	1	Reserved

A6	A5	Drive strength
0	0	Full
0	1	Weak
1	0	Reserved
1	1	Reserved

Figure 11 — Mode Register MR2 definition

3.3.4.1 Thermal Offset

Because of their tight thermal coupling with Wide I/O DRAMs, hot spots on Wide I/O controllers can induce thermal gradients into the DRAMs. As these hot spots may not be located near the DRAM thermal sensor, the DRAM's temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through Mode Register 2 (A16=0, BA1=1, BA0=0) in channel A and it will not be affected through MR2(A0) in channel B, C or D. This temperature offset will modify refresh behavior for all channels in the slice. If the induced thermal gradient from temperature sensor location for DRAM to hot spot location of controller is larger than 15 degrees C, then self-refresh mode will not reliably maintain memory contents. Bit 1 (A1) in MR2 is reserved for future thermal offset use.

During normal operation, the controller will update this register whenever it detects changes in the induced thermal gradient. Since updating this register may modify the self-refresh behavior for all channels, all channels must not be in self-refresh mode when this register is written in channel A.

If changes to the thermal offset indicate that the self refresh frequency increases (that is, the time between refreshes decreases), the memory must reflect these changes immediately. If changes to the thermal offset indicate that the self refresh frequency decreases (that is, the time between refreshes increases), the controller cannot put the memory into self refresh until the controller has refreshed all memory on the device.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor must be located in a predictable location. To provide maximum flexibility, several locations on the memory die are supported. The supported locations are TBD. The specific location used by an individual memory die is indicated by 3 bits in the memory status register. All memory dice in a stack must use the same thermal X-Y location.

To ensure that the memory thermal sensor is located above an X-Y location on the controller, the memory thermal sensor must be located within a rectangle centered on the memory-controller physical interface. Additionally, the minimum size of a controller that wants to use this feature is within that rectangle as otherwise the memory's thermal sensor could be located outside the controller die's perimeter.

3.3.4.2 Drive Strength

Drive strength can be set to full or weak strength via address bits A5 and A6.

Full strength supports 3pF channel load and weak strength supports 2pF channel load to achieve minimum slew rates of 1V/ns.

3.3.4.3 nWR

This is used to program internal auto precharge start timing for Write with auto precharge command.

$$nWR \geq RU(tWR/tCK)$$

3.3.5 Mode Register MR3

The mode register MR3 is used for partial array self refresh.

Table 9 — Mode Register MR3 definition

A16	BA1	BA0	A15 -A0
0	1	1	PASR

Table 10 — Bank/Segment mask definition for PASR

Monolithic die density				1Gb	2Gb	4Gb		8Gb		16Gb		32Gb
MR#	MR bit	PASR Mask Area		BA1:0	BA1:0	BA1:0	RA13	BA1:0	RA14:13	BA1:0	RA14:12	
MR3	A0	Bank0	Segment0	00B	00B	00B	0B	00B	00B	00B	000B	TBD
	A1	Bank1		01B	01B	01B	0B	01B	00B	01B	000B	
	A2	Bank2		10B	10B	10B	0B	10B	00B	10B	000B	
	A3	Bank3		11B	11B	11B	0B	11B	00B	11B	000B	
	A4	Bank0	Segment1	-	-	00B	1B	00B	01B	00B	001B	
	A5	Bank1		-	-	01B	1B	01B	01B	01B	001B	
	A6	Bank2		-	-	10B	1B	10B	01B	10B	001B	
	A7	Bank3		-	-	11B	1B	11B	01B	11B	001B	
	A8	Bank0	Segment2	-	-	-	-	00B	10B	00B	010B	
	A9	Bank1		-	-	-	-	01B	10B	01B	010B	
	A10	Bank2		-	-	-	-	10B	10B	10B	010B	
	A11	Bank3		-	-	-	-	11B	10B	11B	010B	
	A12	Bank0	Segment3	-	-	-	-	00B	11B	00B	011B	
	A13	Bank1		-	-	-	-	01B	11B	01B	011B	
	A14	Bank2		-	-	-	-	10B	11B	10B	011B	
	A15	Bank3		-	-	-	-	11B	11B	11B	011B	

3.3.5.1 Partial Array Self Refresh (PASR)

With Partial Array Self Refresh (PASR), the self refresh may be restricted to a variable portion of the total array. The PASR detail scheme will be defined. Data outside the defined area will be lost. Address bits A0 to A15 are used to set PASR. When the bit is programmed 0, refresh operation to the corresponding area will not be blocked (not masked) and will be refreshed.

3.3.6 Mode Register MR5

3.3.6.1 Rank-to-Rank DQ/DQS Tuning

Wide I/O DRAMs must provide rank-to-rank timing accuracy to within 500ps between ranks across PVT. To enable this, Wide I/O DRAMs insert variable delays into their DQ and DQS generation circuits. In addition, Wide I/O controllers have phase discrimination circuits that can determine, within 100ps, the relative arrival times of two pulses on different DQ lines.

DRAM delay step size is not specified. The DRAM design should set the maximum step size to ensure that once alignment has been achieved, the ranks will stay aligned within 500ps across all subsequent operating conditions, i.e., as voltage and temperature within the DRAM stack changes. To achieve this, the DRAM may specify conditions that will require subsequent retuning. The DRAM design should set the minimum step size and step count to ensure that enough delay can be inserted into the fastest devices to align their DQ and DQS timing with the slowest devices.

Different delays can be inserted into the DQ generation circuits and the DQS generation circuits as DQ delays are from the rising edge of CK while DQS delays are from the falling edge of CK. This can be used to account for different sampling points for the rising and falling edges for CK in the memory devices to ensure DQS edges are more closely centered within the data eye.

Within a rank, the inserted DQ delay is the same for all DQ outputs. Within a rank, the inserted DQS delay is the same for all DQS outputs. Within a slice, each channel has independent delay elements and controls.

During initialization, the Wide I/O controller tells each rank in the memory system to place continuous CK/2 pulses on different DQ and DQS signals. The controller then tells each memory rank to insert delays into the DQ/DQS circuits until all channels' pulses align within the accuracy of the controller's phase discriminator.

DRAM vendors have the option of performing this tuning at the time of memory manufacture. If this is done, then tuning is not required at system initialization and the memory need not provide dynamic tuning functionality.

This functionality is required for all 2-, 3- and 4-slice configurations but is optional in 1-slice configurations.

Because this functionality adds delay to memory response, the tAC and tDQSK parameters are specified with zero delay added.

The number of delay steps supported by the memory is in DQ17:16 of the status register:

Table 11 — Delay Steps

DQ17	DQ16	
0	0	no steps (factory tuning)
0	1	8 steps
1	0	16 steps
1	1	32 steps

Control of tuning is through Mode Register 5 (A16=1, BA1=0, BA0=1). Delay insertion for the DQ delay from the positive going edge of CK is shown in the following table:

Table 12 — DQ delay Insertion

A16	BA1	BA0	A1	A0	
1	0	1	0	0	Do not change delay
1	0	1	0	1	Increase +CK to DQ delay 1 element
1	0	1	1	0	Decrease +CK to DQ delay 1 element
1	0	1	1	1	Remove all +CK to DQ delay

Delay insertion for the DQS delay from the negative going edge of CK is shown in the following table:

Table 13 — DQS delay Insertion

A16	BA1	BA0	A3	A2	
1	0	1	0	0	Do not change delay
1	0	1	0	1	Increase -CK to DQS delay 1 element
1	0	1	1	0	Decrease -CK to DQS delay 1 element
1	0	1	1	1	Remove all -CK to DQS delay

In both cases, the delay will be reflected in DRAM timing no more than 10 DRAM clock cycles from the MRS command.

Control of tuning timing pulses is through Mode Register 5 (A16=1, BA1=0, BA0=1). CK/2 means the clock frequency is divided by 2 (the period is doubled). +CK/2 is a divide by 2 where the output edge transition is triggered by a rising edge of CK. -CK/2 is a divide by 2 where the output edge transition is triggered by a falling edge of CK. To ensure that the training pulses are in phase, the mode register 5 writes must be sent on even clock boundaries, that is, if the MR5 write to rank 0 is sent on clock 0, the MR5 writes to rank 1, 2 and 3 must be sent on clocks 2, 4, 6 or so on.

During training mode, DQ/DQS not specified must be floated so as to not create contention within the memory stack.

Table 14 — Control of Tuning Timing Pulses

A16	BA1	BA0	A7	A6	A5	A4	
1	0	1	0	0	0	1	place +CK/2 on DQ8, -CK/2 on DQS0
1	0	1	0	0	1	0	place +CK/2 on DQ24, -CK/2 on DQS1
1	0	1	0	1	0	0	place +CK/2 on DQ40, -CK/2 on DQS2
1	0	1	1	0	0	0	place +CK/2 on DQ56, -CK/2 on DQS3
1	0	1	0	0	0	0	normal DQ/DQS functionality

3.3.6.2 Sample Timing Tuning Sequence

The sequence to align timing between ranks must be followed for each channel. At a high level the sequence is as follows:

Check to see whether all devices in the rank need DQ/DQS tuning by examining the appropriate bits in the status register. Continue only if DQ/DQS tuning is necessary.

Reset the delay to zero for each device in the channel.

Tell each rank to place the DQ and DQS training pulses on different DQ and DQS micropillars, e.g., tell rank 0 to put the pulses on DQ8/DQS0, tell rank 1 to put pulses on DQ24/DQS1, etc.

Determine which rank's DQ pulses are latest using the controller's phase discriminator.

Have the controller generate an internal reference DQS (-CK/2) clock from the latest rank's DQ pulses. This reference clock operates at DQ frequency but with edges centered at the center of the DQ high and low times, e.g., 90 degrees out of phase with the DQ pulses.

Add delay to the slowest DQ rank and reset the reference DQS clock until all memories' DQS pulses are ahead of or equal to the reference DQS clock.

Add delays to all other DQ clocks until all are aligned with the slowest DQ.

Add delays to all other DQS clocks until all are aligned with the reference DQS.

Restore normal DQ/DQS functionality and stop the reference DQS generator.

3.3.6.3 Sample Tuning Sequence Flow Chart

Below is a flowchart for a sample timing tuning flowchart.

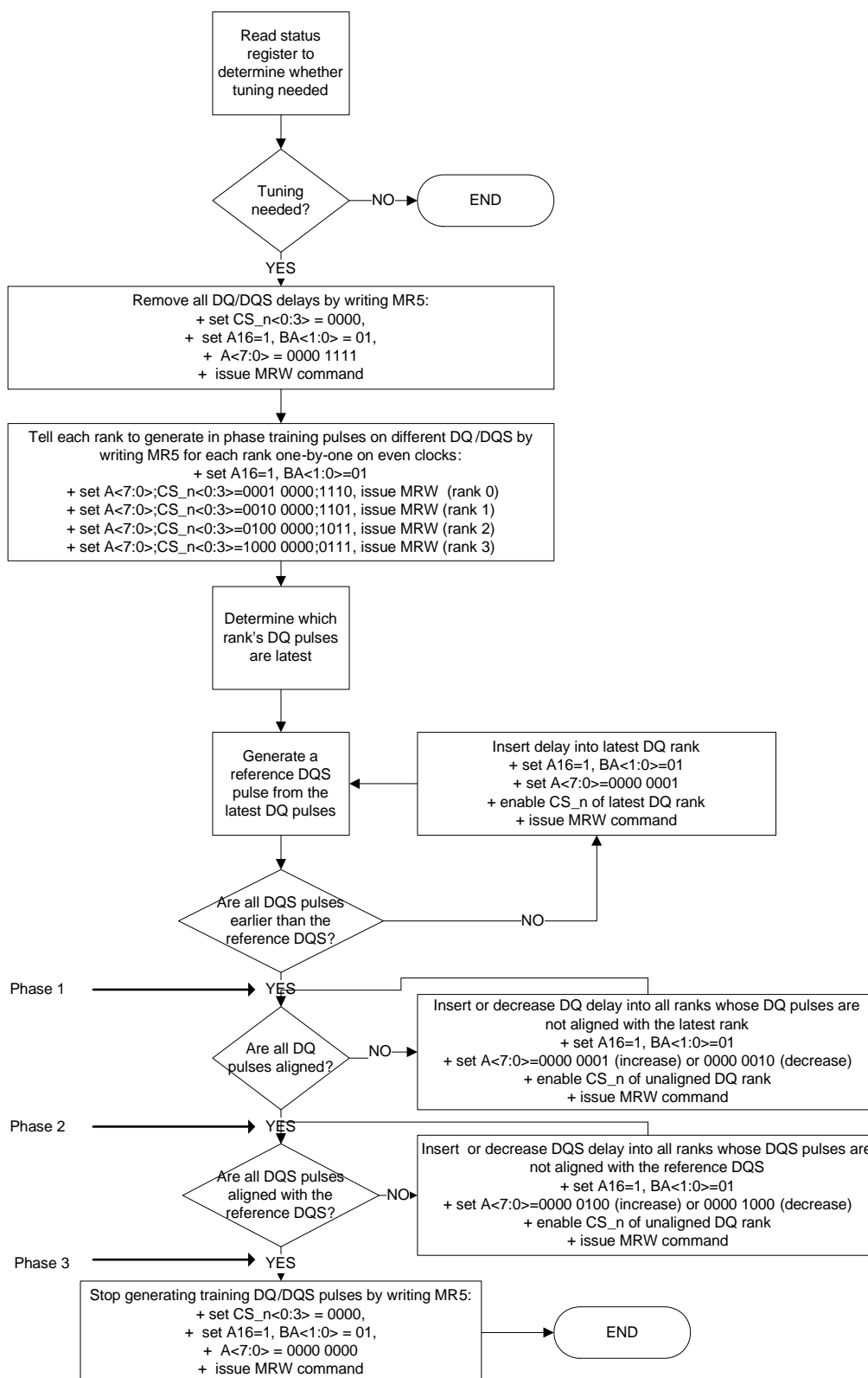


Figure 12 — Sample tuning sequence flowchart

Below are a set of idealized waveforms for the different phases of DQ/DQS tuning. The initial phase shows the starting state when none of the waveforms are aligned:

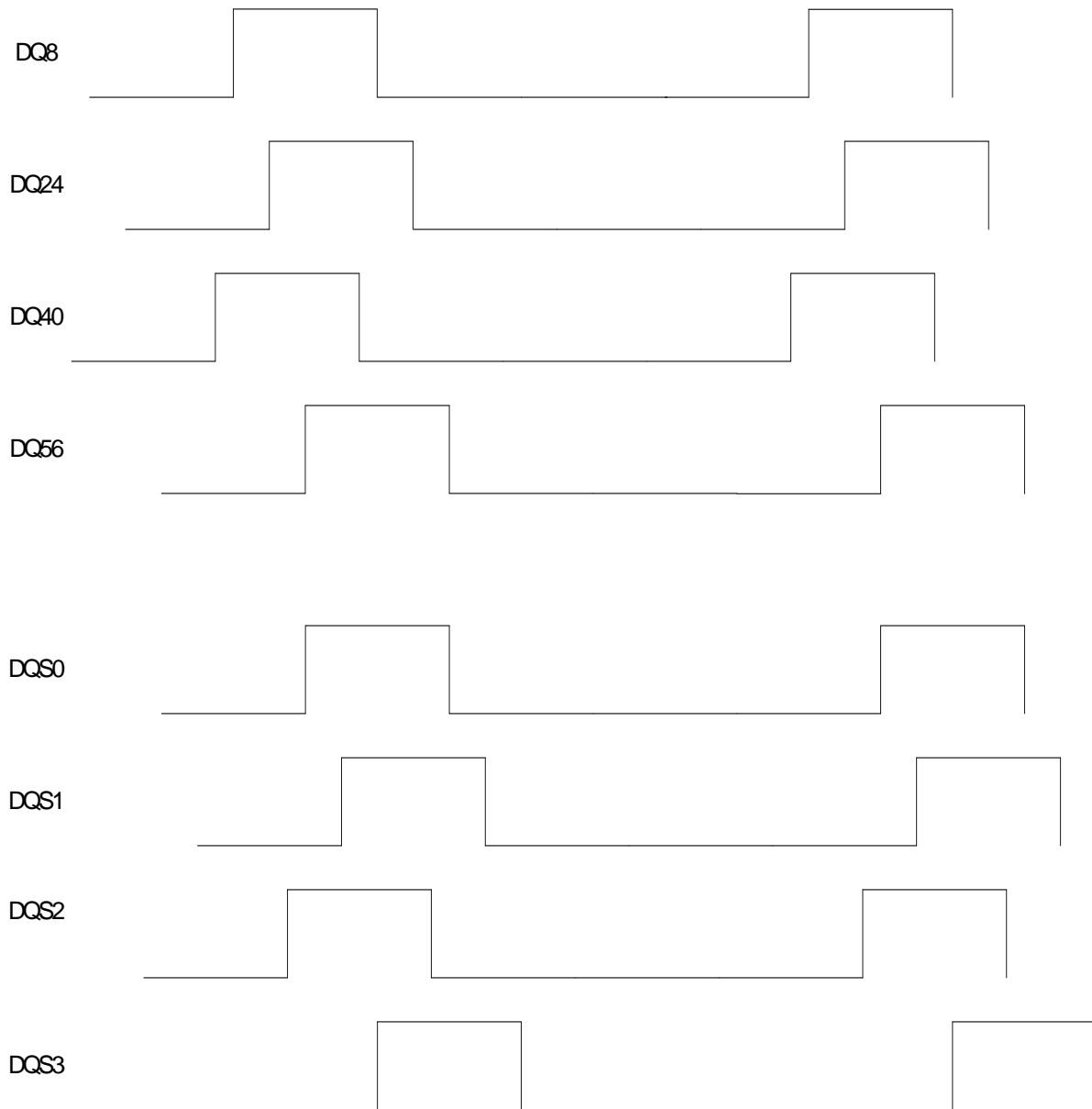


Figure 13 — “Phase 0” of DQ/DQS Tuning

This second diagram shows “phase 1” in the flowchart. This is after the latest DQ is determined, a reference DQS is generated (internal to the controller) and after that reference DQS is determined to be later than all DQS generated by the 4 DRAM ranks:

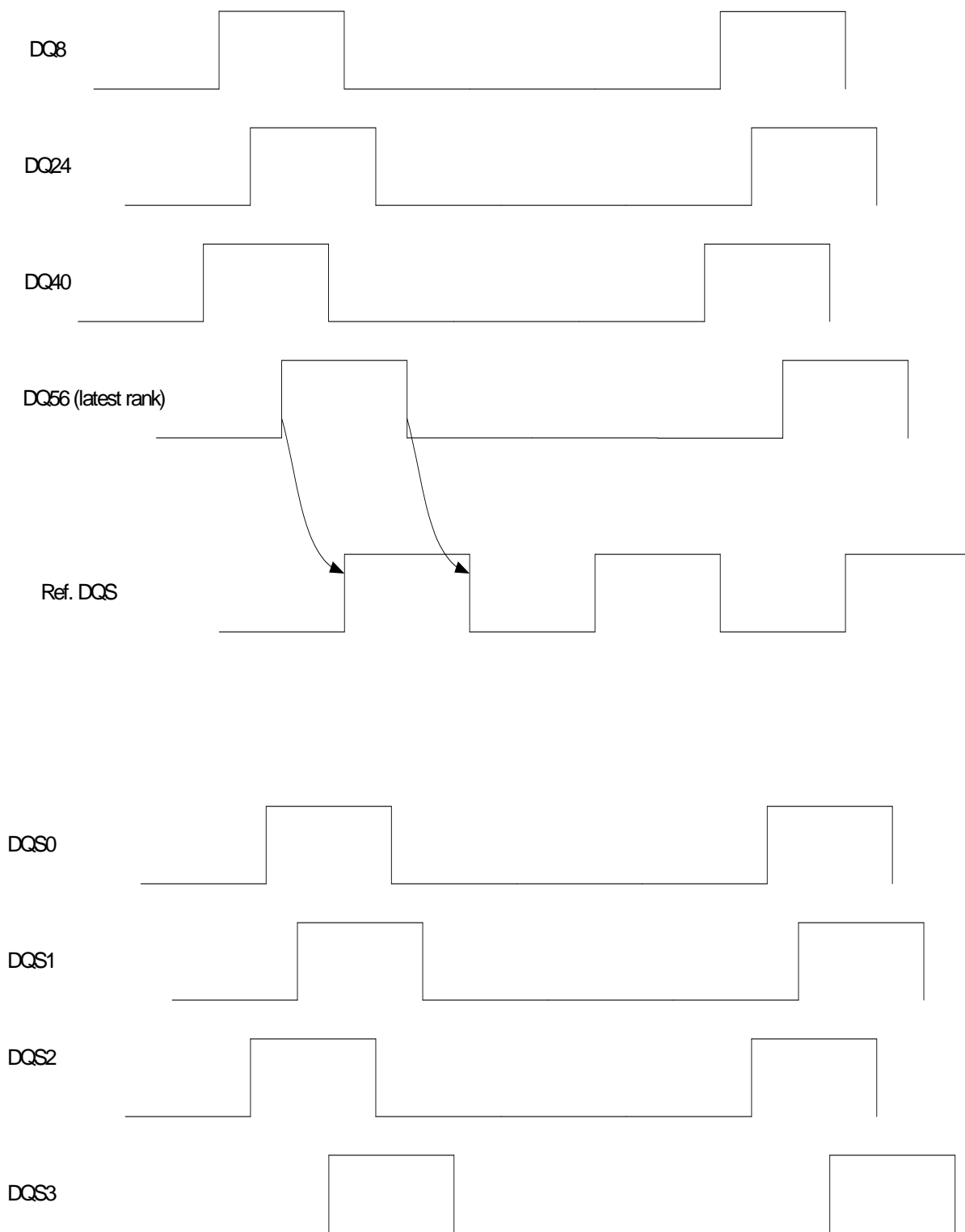


Figure 14 — “Phase 1” of DQ/DQS Tuning

The third diagram shows “phase 2” in the flowchart, after all the earlier DQ are aligned with the latest arriving DQ:

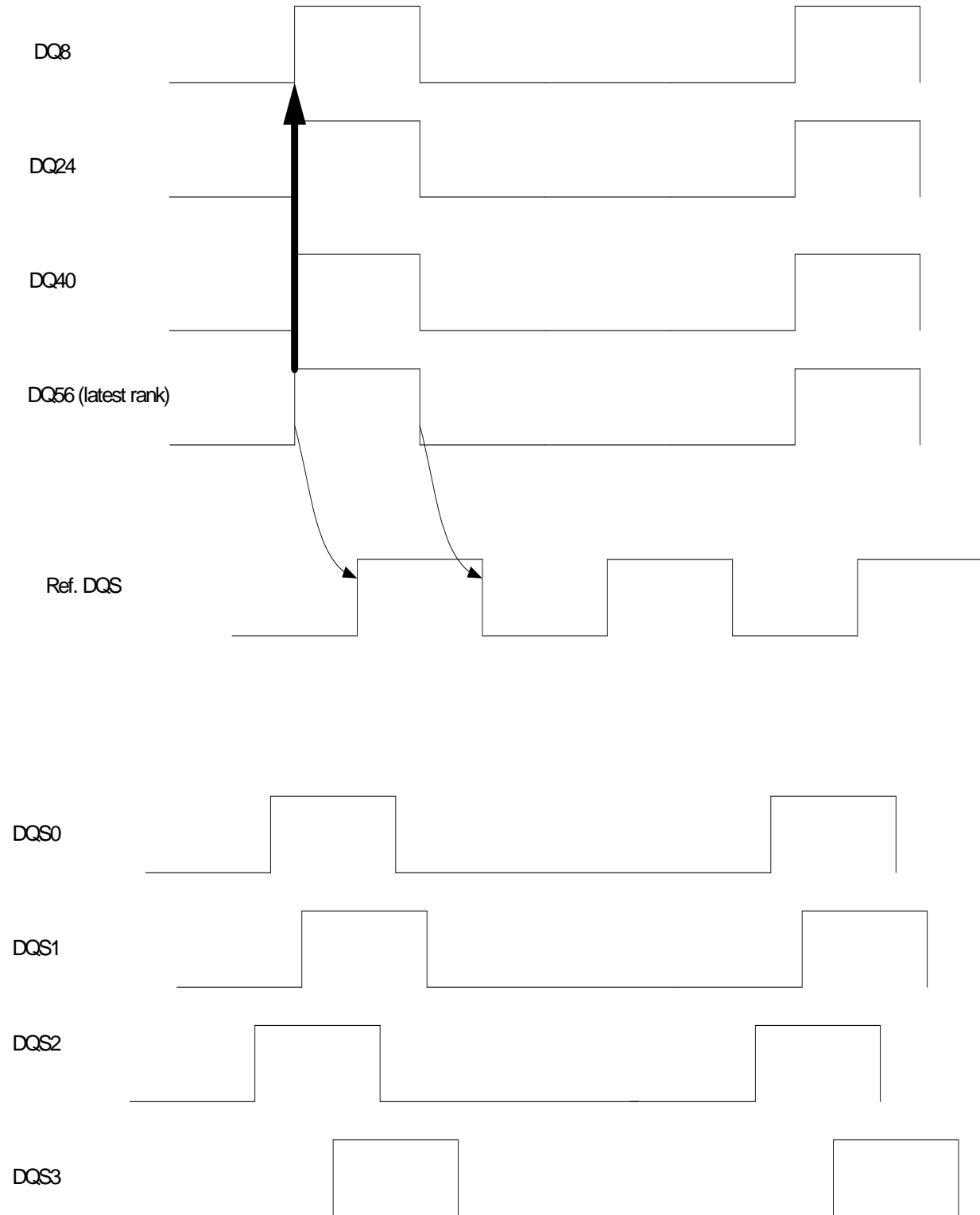


Figure 15 — “Phase 2” of DQ/DQS Tuning

The final diagram shows “phase 3” from the flowchart, after all the DQS from the memory devices are aligned to the controller’s internal reference DQS.

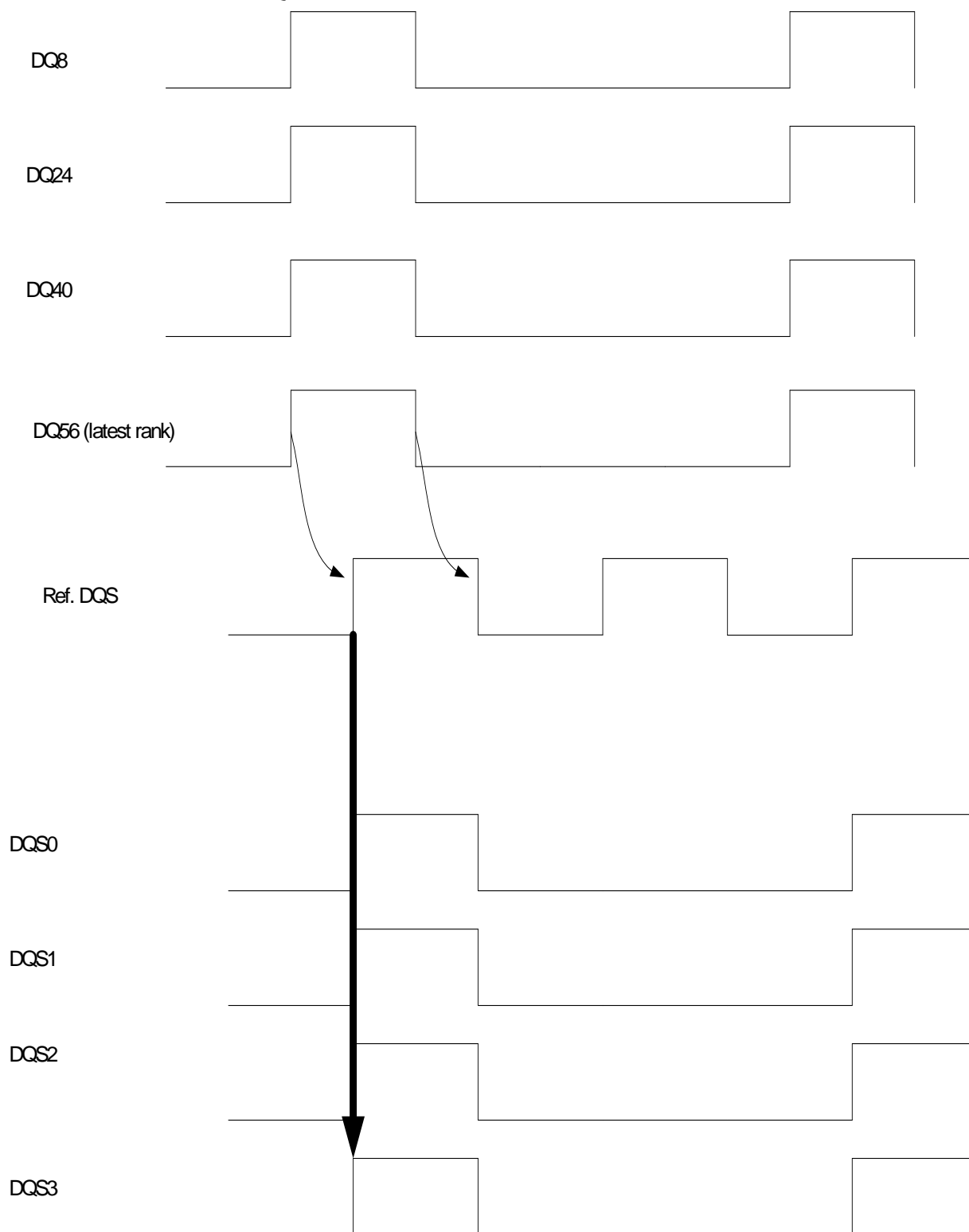


Figure 16 — “Phase 3” of DQ/DQS Tuning

3.3.7 Mode Register MR7

The mode register MR7 is used for partial array self refresh.

Table 15 — Mode Register MR7 definition

A16	BA1	BA0	A15 -A0
1	1	1	PASR

Table 16 — Bank/Segment mask definition for PASR

Monolithic die density				1Gb	2Gb	4Gb		8Gb		16Gb		32Gb
MR#	MR bit	PASR Mask Area		BA1:0	BA1:0	BA1:0	RA13	BA1:0	RA14:13	BA1:0	RA14:12	
MR7	A0	Bank0	Segment4	-	-	-	-	-	-	00B	100B	TBD
	A1	Bank1		-	-	-	-	-	-	01B	100B	
	A2	Bank2		-	-	-	-	-	-	10B	100B	
	A3	Bank3		-	-	-	-	-	-	11B	100B	
	A4	Bank0	Segment5	-	-	-	-	-	-	00B	101B	
	A5	Bank1		-	-	-	-	-	-	01B	101B	
	A6	Bank2		-	-	-	-	-	-	10B	101B	
	A7	Bank3		-	-	-	-	-	-	11B	101B	
	A8	Bank0	Segment6	-	-	-	-	-	-	00B	110B	
	A9	Bank1		-	-	-	-	-	-	01B	110B	
	A10	Bank2		-	-	-	-	-	-	10B	110B	
	A11	Bank3		-	-	-	-	-	-	11B	110B	
	A12	Bank0	Segment7	-	-	-	-	-	-	00B	111B	
	A13	Bank1		-	-	-	-	-	-	01B	111B	
	A14	Bank2		-	-	-	-	-	-	10B	111B	
	A15	Bank3		-	-	-	-	-	-	11B	111B	

3.3.7.1 Partial Array Self Refresh (PASR)

With Partial Array Self Refresh (PASR), the self refresh may be restricted to a variable portion of the total array. The PASR detail scheme will be defined. Data outside the defined area will be lost. Address bits A0 to A15 are used to set PASR. When the bit is programmed 0, refresh operation to the corresponding area will not be blocked (not masked) and will be refreshed.

4 Command Definitions and Timing Diagrams

4.1 Active

The SDRAM Activate command is issued by holding CS_n LOW, RAS_n LOW, and CAS_n HIGH, WE_n HIGH at the rising edge of the clock. The bank addresses BA0 - BA1 are used to select the desired bank. The row address is used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The Wide I/O DRAM can accept a read or write command at time t_{RCD} after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP} , respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Activate commands to different banks is t_{RRD} . No more than 2 banks may be activated in a rolling t_{TAW} window.

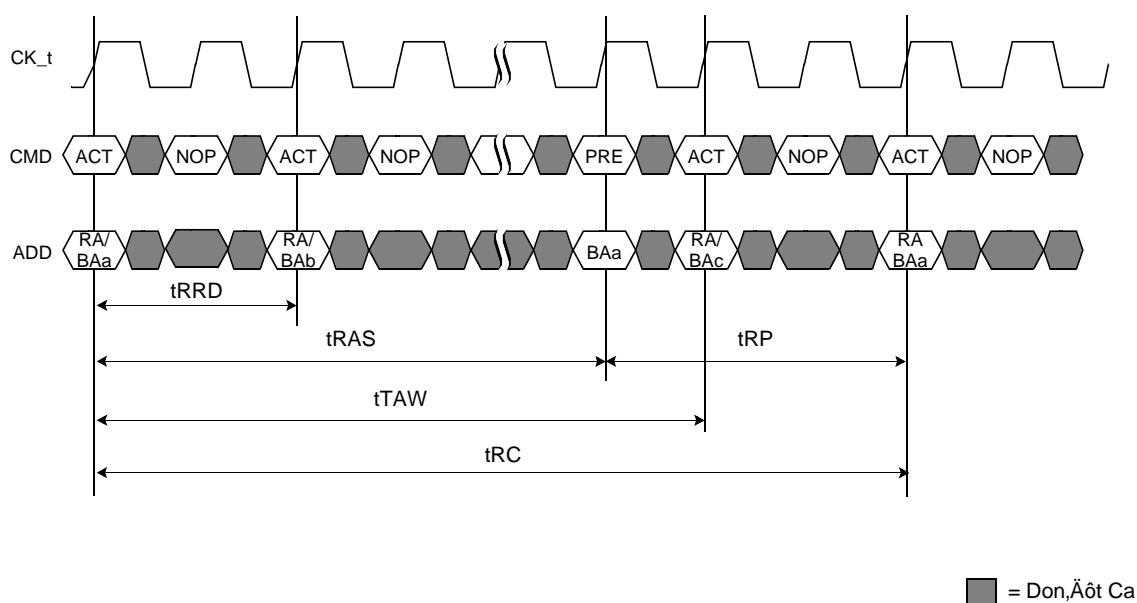
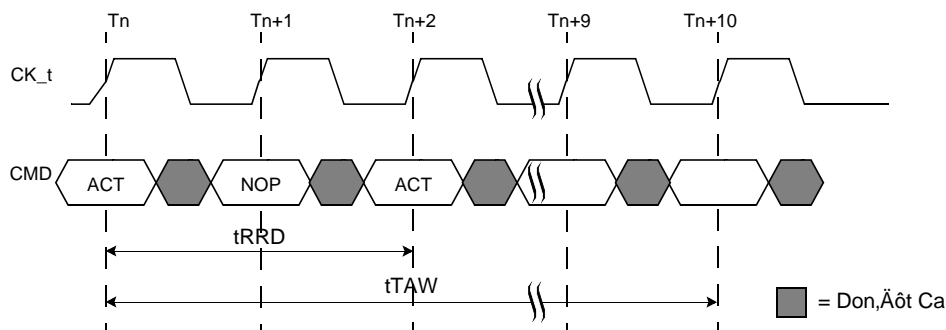


Figure 17 — Active Command

No more than 2 banks may be activated in a rolling t_{TAW} window. Converting to clocks is done by dividing $t_{TAW}[ns]$ by $t_{CK}[ns]$, and rounding up to next integer value. As an example of the rolling window, if $\text{RU}\{ (t_{TAW} / t_{CK}) \}$ is 10 clocks, and an activate command is issued in clock n , only one activate commands may be issued at or between clock $n+1$ and $n+9$.

t_{TAW} is per channel on a single slice restriction.



Example for 200MHz: Two Activate commands allowed between T_n and T_{n+9} .

Figure 18 — Sequential Bank Activation Restriction

4.1 Active (cont'd)

Table 17 — Two bank Activate Window Timing

Parameter	Symbol	Min	Max	Unit
Two Bank Activate window	tTAW	50	-	ns

4.2 Read Operation

4.2.1 Read

The READ command is used to initiate a burst read access to an active row with a burst length as set in the Mode Register. BA0 and BA1 select the bank and the address inputs select the starting column location. The value of A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of the read burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses.

The basic Read timing parameters for DQs are shown in Figure 19 —.

The controller indicates read with full preamble by driving A11 low when signalling a read command. The controller indicate read with short preamble by driving A11 high when signalling a read command.

During Read bursts, DQS is driven by the Wide I/O DRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble. The first data-out element is center aligned with the first rising edge of DQS and the successive data-out elements are center aligned to successive edges of DQS. This is shown in Figure 2 with a READ latency of 3. Upon completion of a read burst, assuming no other READ command has been initiated, the DQs will go to High-Z.

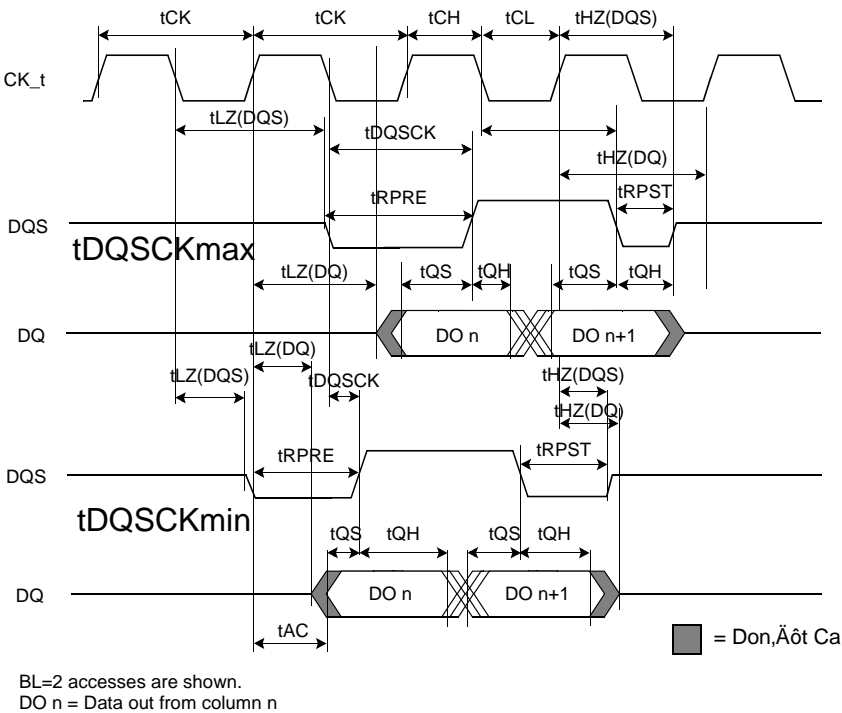


Figure 19 — Basic Read Timing Parameters

4.2.1 Read (cont'd)

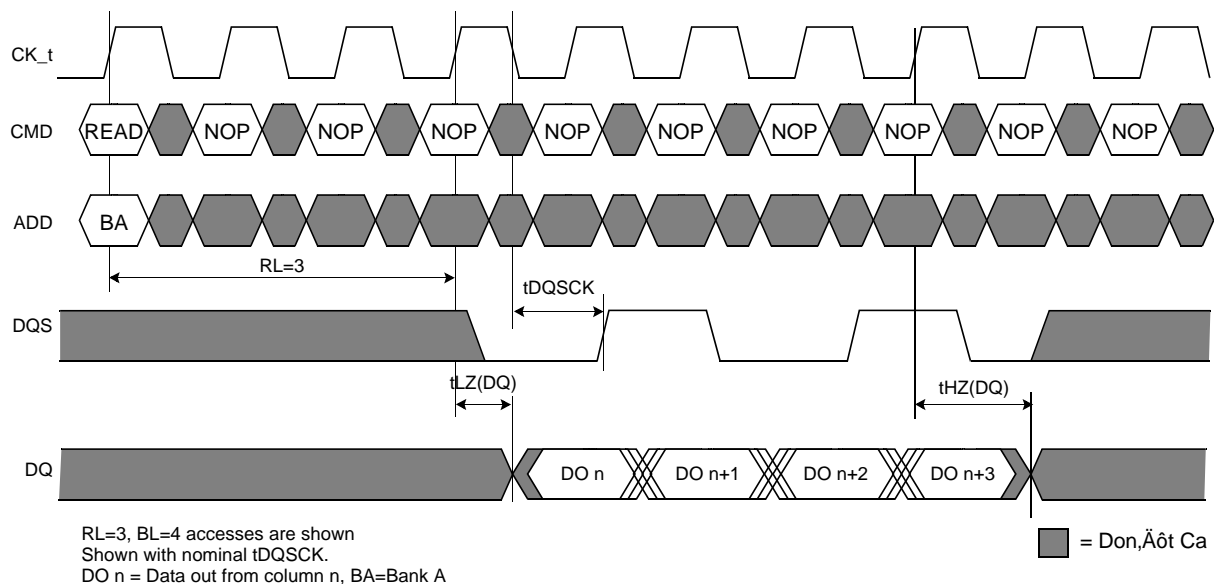


Figure 20 — Read Burst Showing Read Latency

4.2.2 Read to Read (same rank)

Data from a read burst may be concatenated or truncated by a subsequent READ command only when no auto precharge command has been issued. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out elements. X is limited to $2n$, where n is an integer.

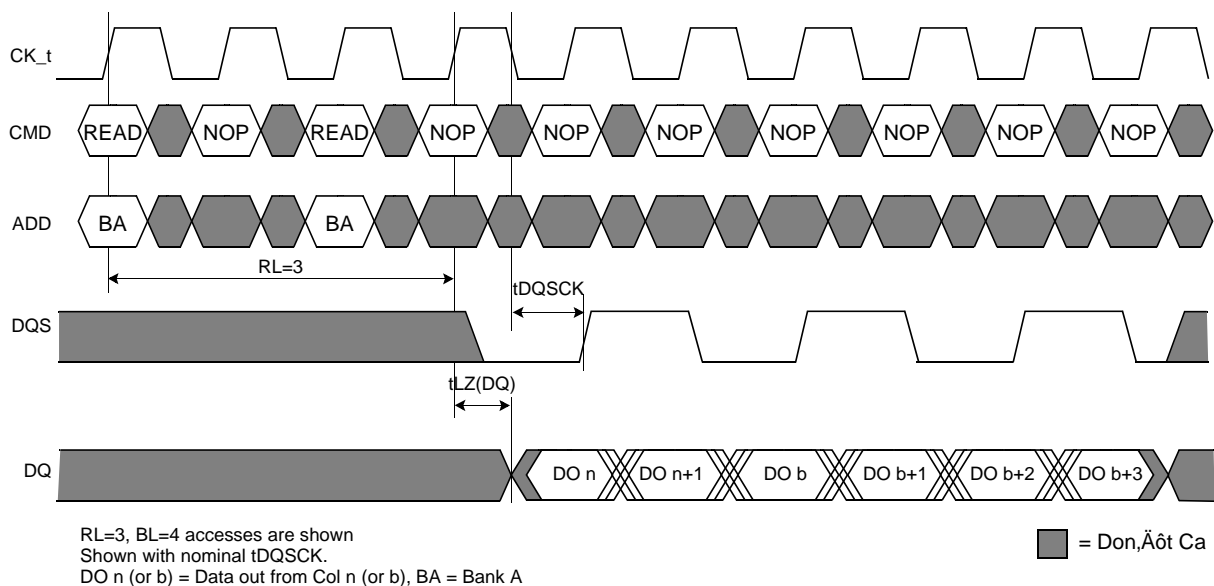


Figure 21 — Read to Read command interval (same rank)

4.3 DQS Timing

DQS will have the following timing values as related to CK timing parameters.

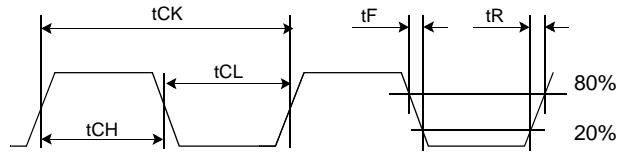


Figure 22 — Clock Timing Definition

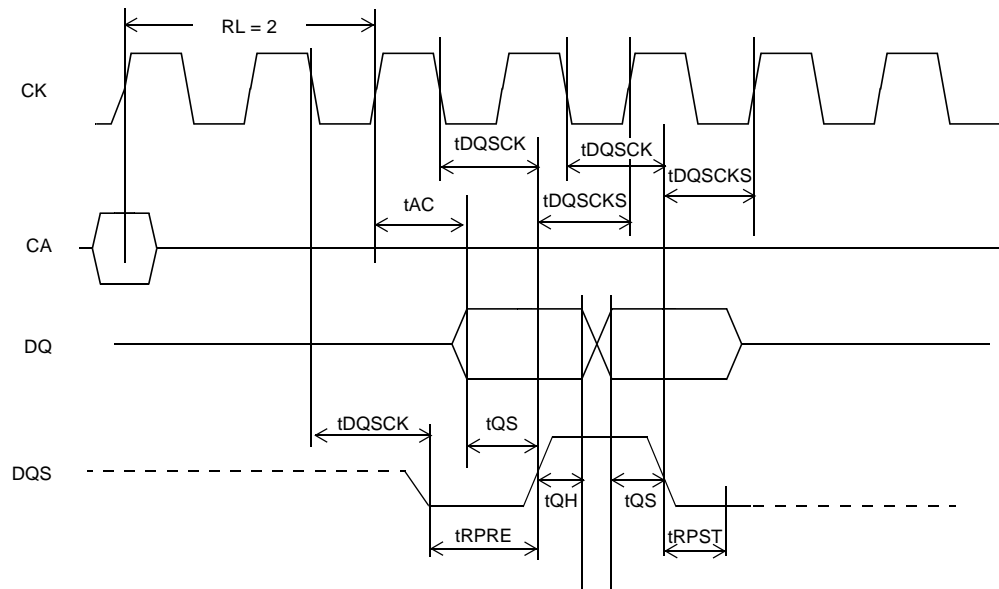


Figure 23 — DQS related timing Definition

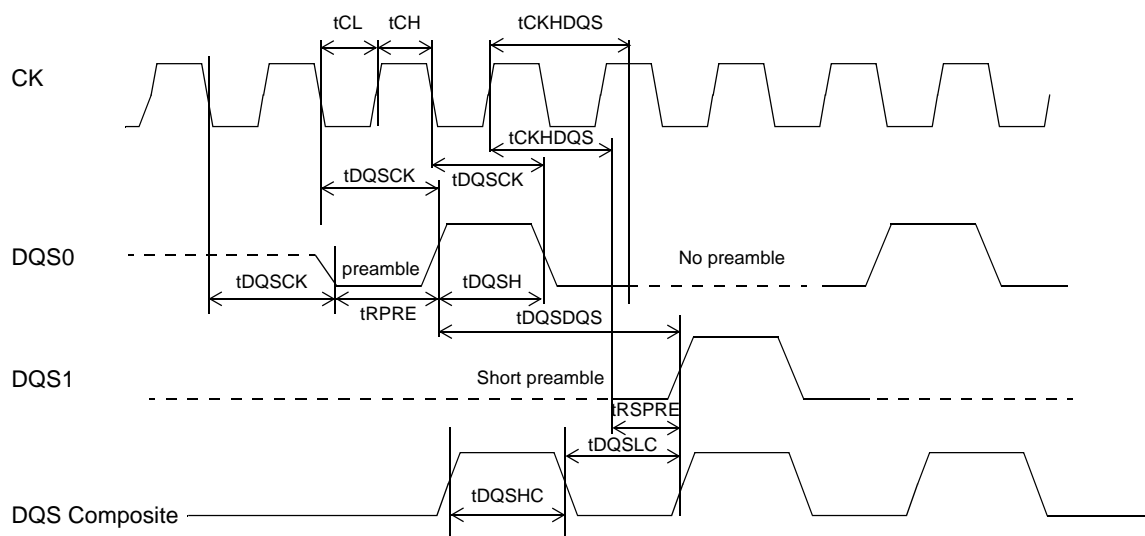


Figure 24 — DQS Composite timing Definition

4.3 DQS Timing (cont'd)

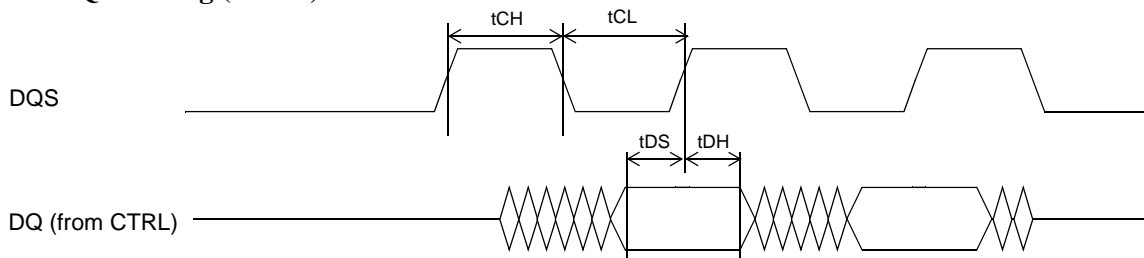


Figure 25 — Write timing Definition

4.4 Read With Short Preamble

To support zero-bubble rank-to-rank, back-to-back read cycles, Wide I/O DRAMs support read with both full and short preambles. During a read with full preamble (that is, a normal read), the Wide I/O DRAM will drive DQS low at the beginning of the clock immediately preceding its first data transfer if it was not already driving DQS for a previous read. During a read with short preamble, the Wide I/O DRAM will also begin driving DQS low in the clock before the first data transfer but only after a time such that it will not fight with another DRAM driving DQS high.

Read with short preamble must be used when the controller is requesting a read from a second DRAM rank where there is no bubble between a previous read from a first DRAM rank. If the second DRAM rank were to drive a full preamble, its preamble might contend with the DQS from the last data transfer of the first DRAM rank.

In the case of back-to-back reads within the same rank, the second read within the same rank can be signalled by either a normal read command or by a read with short preamble command.

The controller indicates a read with normal preamble by driving A11 low when signalling a read command. The controller indicates a read with short preamble by driving A11 high when signalling a read command. This is similar to how it indicates a read with or without precharge.

Read with short preamble can indicate autoprecharge.

Read with short preamble without autoprecharge will be indicated by the acronym: RSP. Read with short preamble with autoprecharge will be indicated by the acronym: RSPA.

4.5 DQ/DQS Contention During Zero-Bubble Back-to-Back Reads from Different Ranks

4.5.1 Rank-to-Rank Switching

Multirank Wide I/O DRAM devices will support zero-bubble rank-to-rank read switching with no DQ or DQS contention even if the AC timing parameters would seem to indicate otherwise. When requesting a read from one rank where another rank was driving DQS/DQ in the clock immediately before the first clock of the requested read, the controller must signal a read-with-short-preamble command to the second rank to tell the second rank that it should drive a short preamble on DQS so as to not contend with the final DQS transition from the first rank. The multiple chips comprising the multiple DRAM ranks will ensure that DQS will not glitch or float during zero-bubble rank-to-rank reads.

4.6 Write Operation

4.6.1 Write

The WRITE command is used to initiate a burst write access to an active row with a burst length as set in the Mode Register. BA0 and BA1 select the bank and the address inputs select the starting column location. The value of A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected, the row being accessed will be precharged at the end of the write burst; if Auto Precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the data bus is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored and a write will not be executed to that byte / column location.

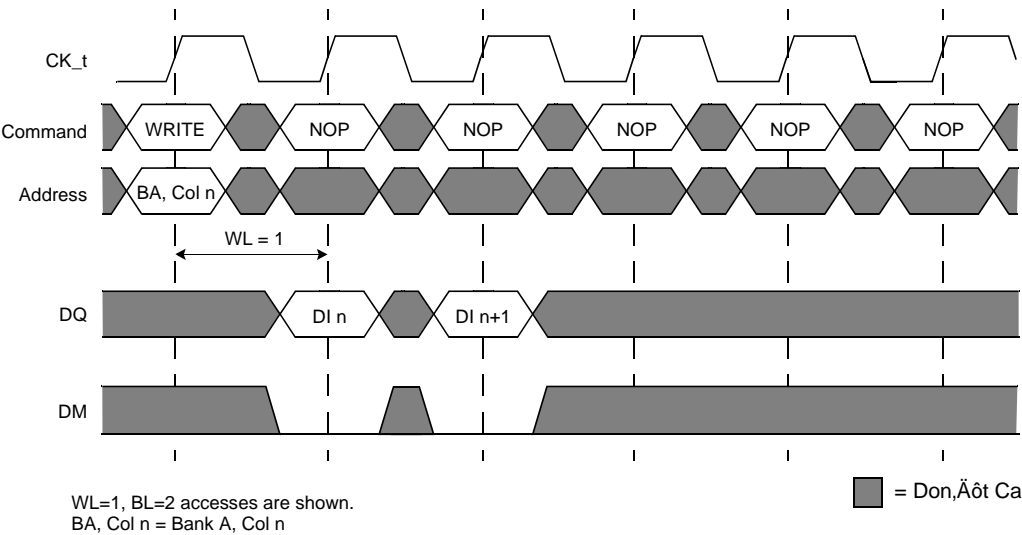


Figure 26 — Burst Write access

4.6.2 Write to Write

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command when no auto precharge command has been issued. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command. The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element.

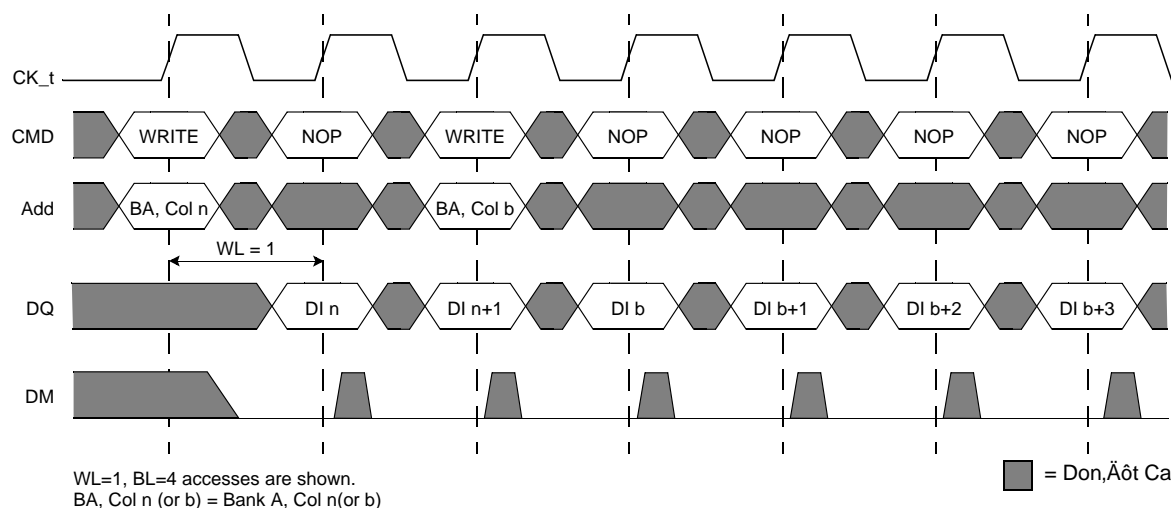


Figure 27 — Write to Write command interval (same rank)

4.7 Read to Write

4.7.1 Read to Write

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. The earliest timing when the WRITE command can be issued is the first rising clock edge after DQ becomes HiZ.

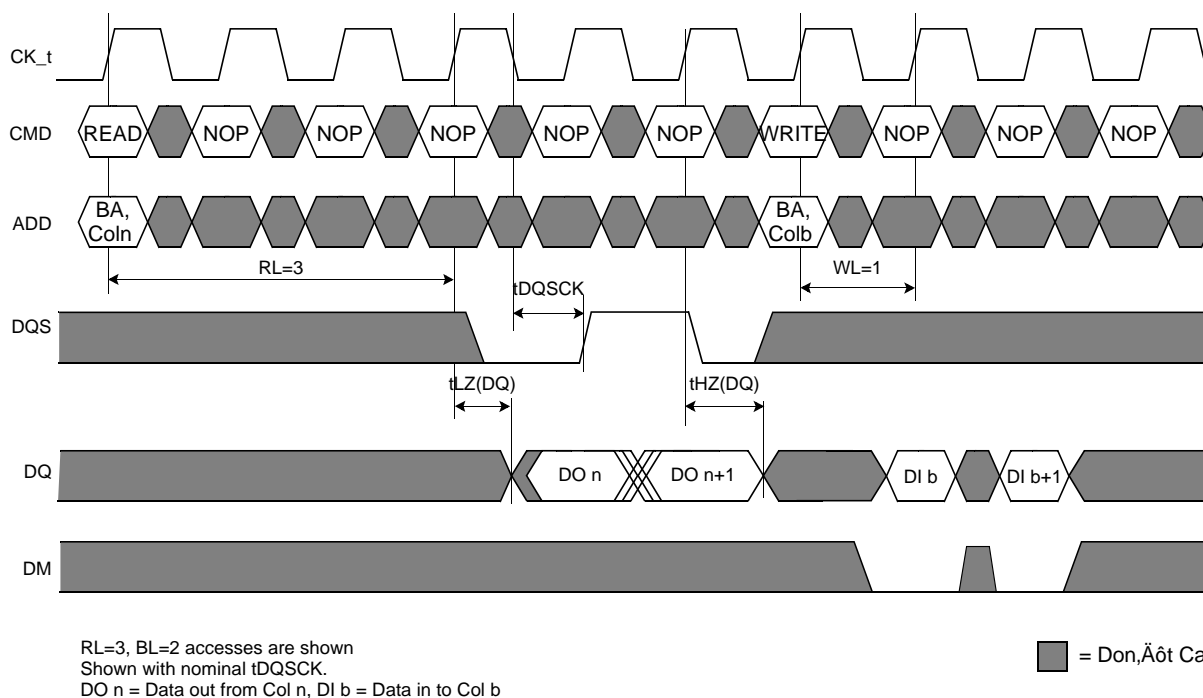
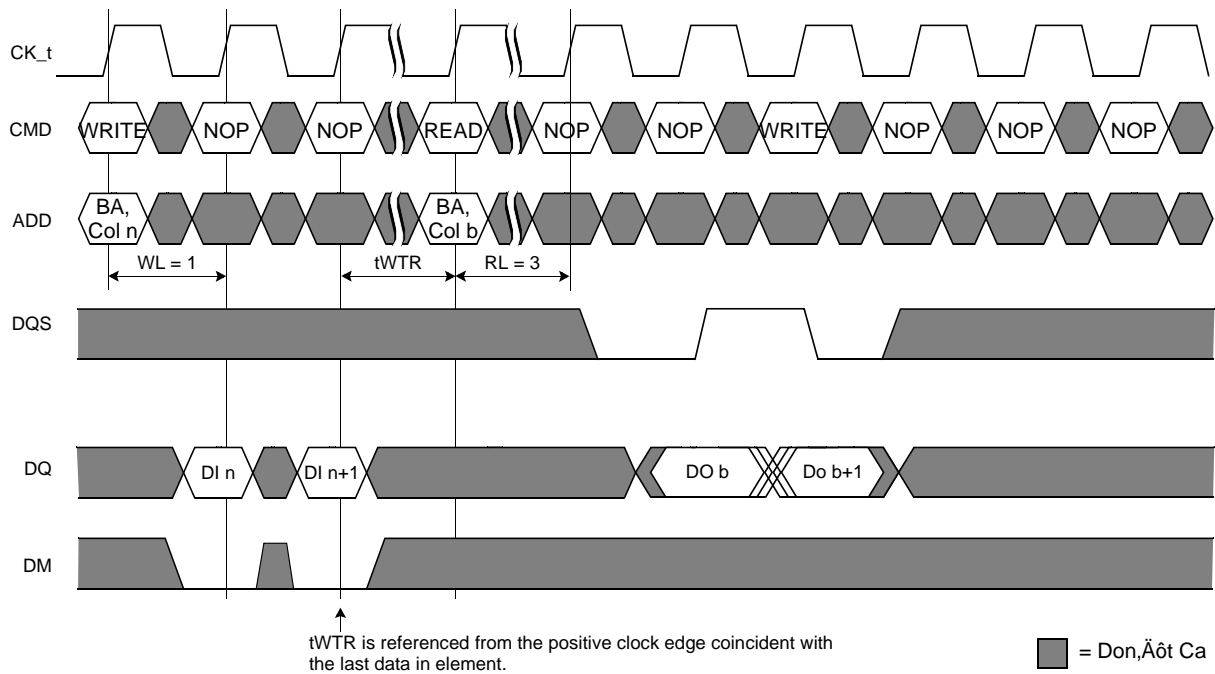


Figure 28 — Read to Write command interval

4.7.2 Write to Read

Data for any Write burst may be followed by a subsequent READ command. To follow a Write, tWTR should be met as shown in Figure 29.

Data for any Write cannot be truncated by a Read command even if data-in element is masked with DM. This means tWTR is always referenced from the rising clock edge coincident with the last data-in element.



RL=3, WL=1, BL=2 accesses are shown
Shown with nominal tDQSCK.
DI n = Data in to Col n, DO b = Data out from Col b

Figure 29 — Write to Read Command Interval

4.8 Burst Terminate

4.8.1 Read Burst Terminate

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the Read latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element. X is limited to $2n$, where n is an integer.

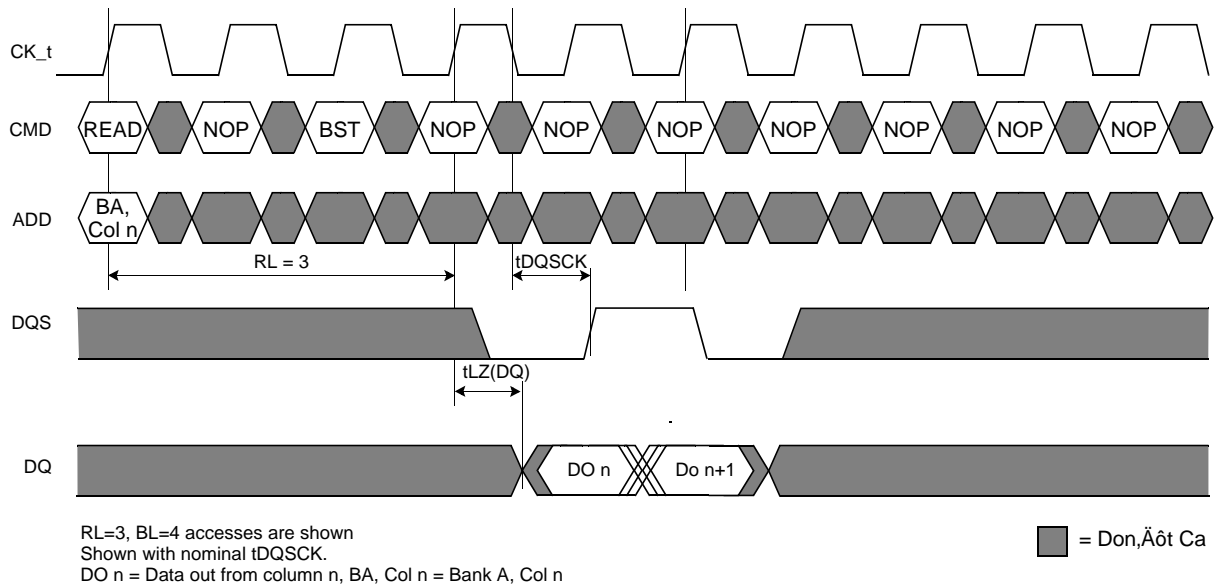


Figure 30 — Read Burst Terminate

4.8.2 Write Burst Terminate

Data from any WRITE burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the Write latency, i.e., the BURST TERMINATE command should be issued X cycles after the WRITE command where X equals the desired data-out element.

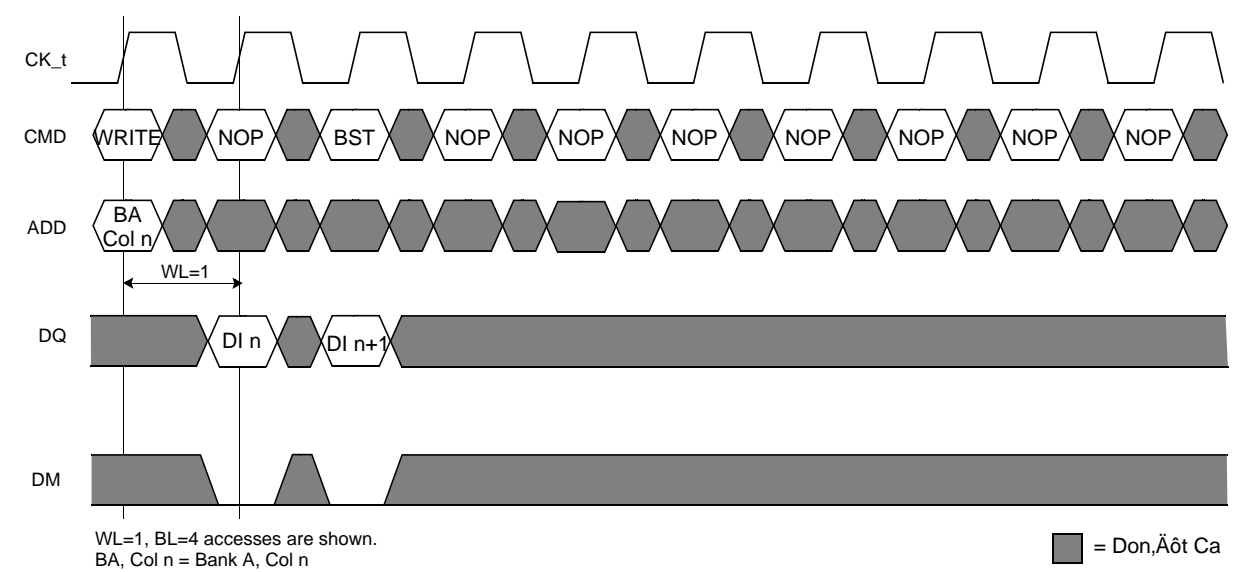


Figure 31 — Write Burst Terminate

4.9 Write Data Mask

No information at this time.

4.10 Precharge and Auto Precharge operation

4.10.1 Read to Precharge

A READ burst cannot be terminated by the PRECHARGE command.

The minimum READ to PRECHARGE command interval (same bank) is Burst Length (BL).

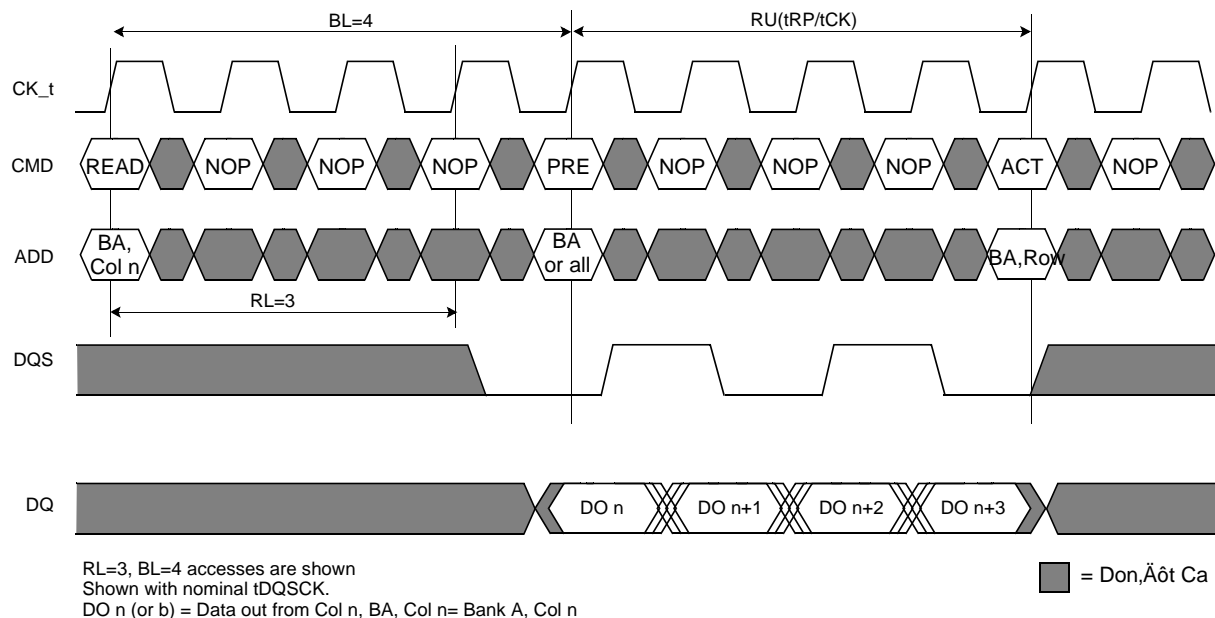


Figure 32 — Read to Precharge command interval (same bank)

4.10.2 Write to Precharge

A WRITE burst cannot be terminated by the Precharge command.

The minimum WRITE to PRECHARGE command interval (same bank) is WL+BL-1+RU(tWR/tCK) cycles.

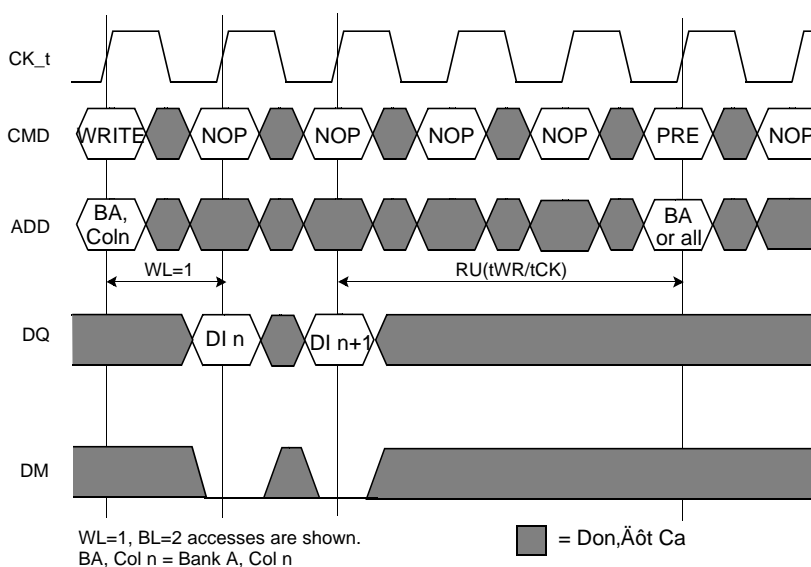


Figure 33 — Write to Precharge command interval (same bank)

4.10.3 Auto Precharge

Auto Precharge is a feature which performs the bank precharge function without requiring an explicit command. This is signalled by driving A10=High) with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent: it is either enabled or disabled for each individual READ or WRITE command.

Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharging time (tRP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time as described for each burst type in the Operation section of this specification.

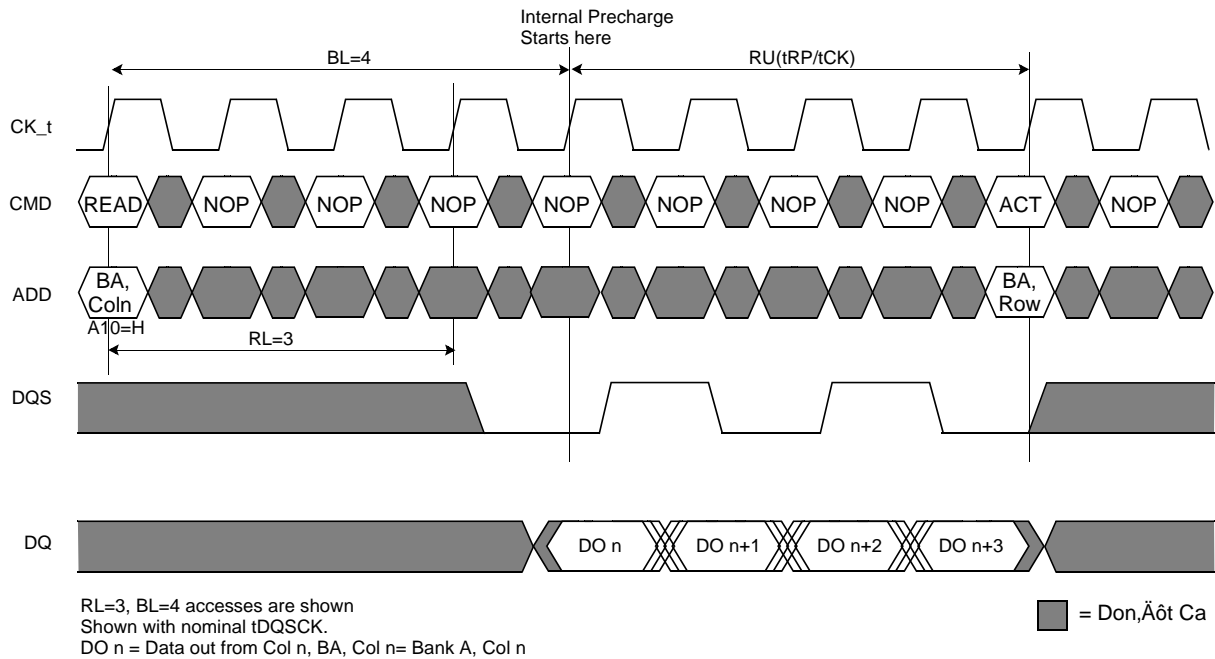


Figure 34 — Read with Autoprecharge

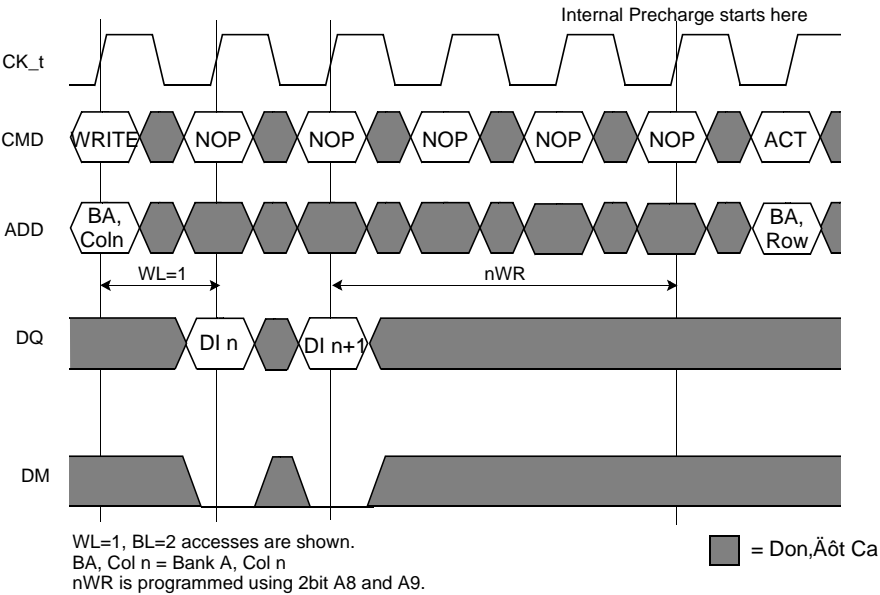


Figure 35 — Write with Autoprecharge

4.11 Auto Refresh

An auto refresh command is issued by having CS_n, RAS_n and CAS_n held low with CKE and WE_n high at the rising edge of the clock (CK). All banks must be precharged and idle for tRP(min) before the auto refresh command is applied. Once this cycle has been started, no control of the external address micropillars are required because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the auto refresh command and the next activate command or subsequent auto refresh command must be greater than or equal to the tRFC(min).

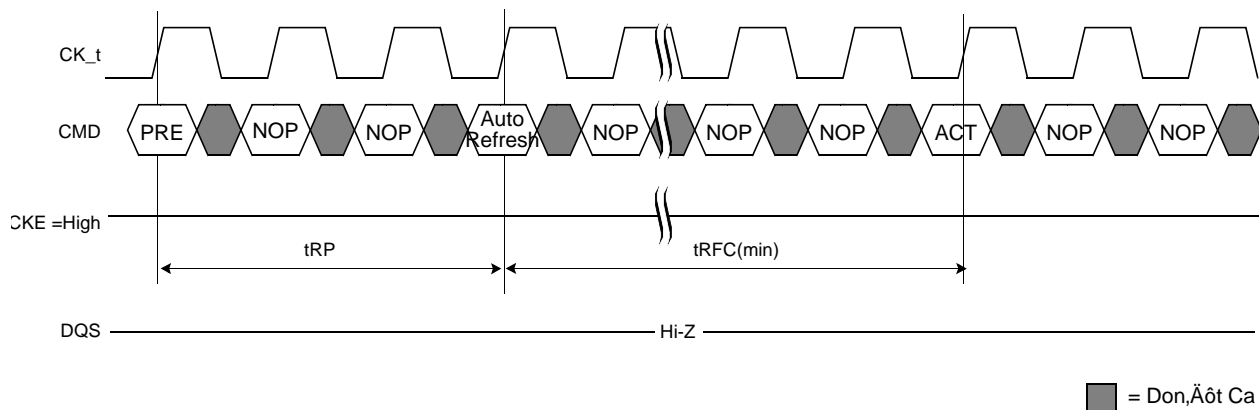


Figure 36 — Auto Refresh Timing

The Auto Refresh command is used during normal operation. This command is non-persistent so it must be issued each time a refresh is required. Refresh addresses are generated by an internal refresh controller.

Regular, distributed refresh pattern is used for Wide I/O DRAM. An Auto Refresh command must be issued at an average periodic interval of tREFI.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed, meaning that the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 9*tREFI.

Postponing Refresh commands may introduce the possibility of violating refresh time tREF.

The number of refresh commands R in any tREF window must always be satisfied.

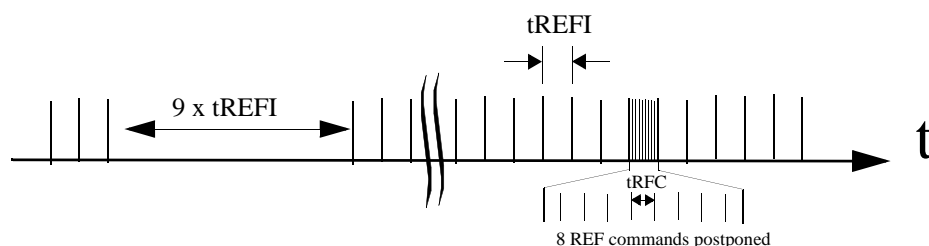


Figure 37 — Postponing Refresh commands (Example)

Table 18 — Refresh Requirement Parameters

Parameter	Symbol	1Gb	2Gb	4Gb	8Gb	Unit	Note
Refresh time	tREF (0 °C ≤ Tc ≤ 85 °C)	64	64	64	64	ms	
Average periodic refresh interval	tREFI (0 °C ≤ Tc ≤ 85 °C)	15.6	7.8	3.9	3.9	us	1
Required number of refresh commands in Refresh time tREF	R	4096	8192	16384	16384		
AUTO REFRESH to ACTIVE / AUTO REFRESH command period	tRFC	90	130	130	210	ns	

NOTE 1 For temperatures above 85 °C, use the refresh rate specified by status register.

4.12 Self Refresh

A Self Refresh command is defined by having CS_n, RAS_n, CAS_n and CKE held low with WE_n high at the rising edge of the clock. Once the self Refresh command is initiated, CKE must be held low to keep the device in Self Refresh mode. After 2 clock cycle from the self refresh command, all of the external control signals including system clock(CK) can be disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. Before returning CKE high to exit the Self Refresh mode, apply stable clock input signal with Deselect or NOP command asserted. The Wide I/O SDRAM initiates a minimum of one all-bank refresh command internally within tCKESR period once it enters Self Refresh mode.

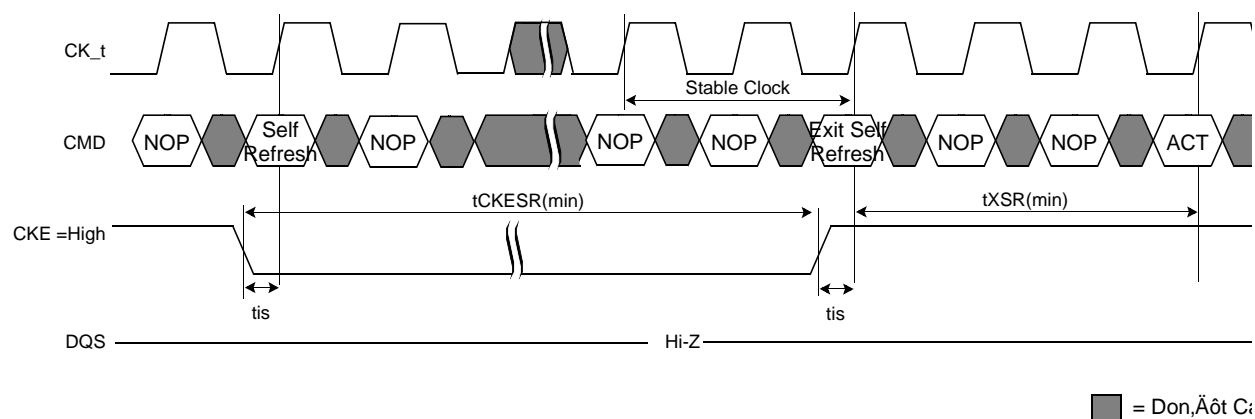


Figure 38 — Self refresh timing

NOTE 1 Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

NOTE 2 Device must be in the all banks idle state prior to entering Self Refresh mode.

NOTE 3 The minimum time that the device must remain in Self Refresh mode is tCKESR.

4.13 Mode Register Write

For application flexibility, various functions, features, and modes are programmable in Wide I/O DRAM Mode Registers. Values are programmed into Mode Registers via a Mode Register Set (MRS) command. The default values of the Mode Registers (MR#) are not defined so they must be programmed during the reset and initialization sequence.

The contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register will be redefined when the MRS command is issued.

MRS commands do not affect array contents regardless of when these commands are executed.

After the mode register set command, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.

The mode registers are divided into various fields depending on the functionality and/or modes.

4.14 Power-Down

Power down scheme support each channel. The device enters power down mode when CKE low, and it exits when CKE high. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. All banks shall be in idle state prior to entering the precharge power down mode and CKE should be set in high for at least t_{XP} prior to Row active command. Refresh operation cannot be performed during power down mode longer than $9 \cdot t_{REFI}$ (minus t_{PDEX} to be accurate). Two stable clocks must be registered prior to Power Down exit.

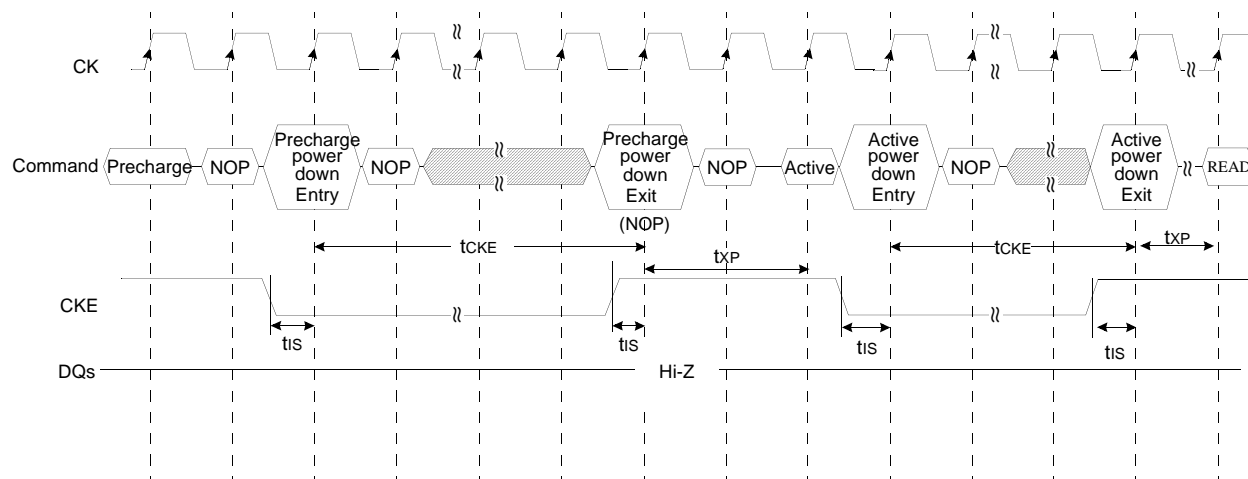
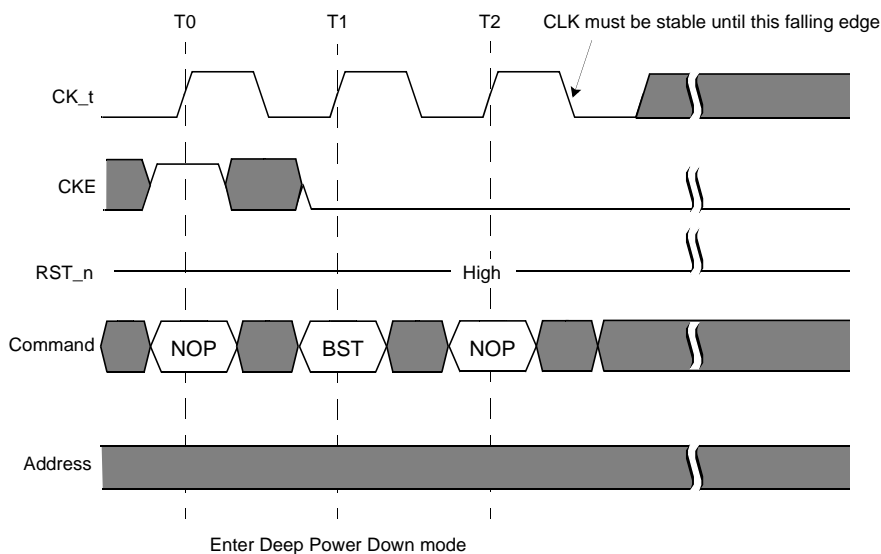


Figure 39 — Power-Down

4.15 Deep Power Down

4.15.1 Deep Power Down Entry



Note

Any channels in a slice is not allowed to stay at DPD state individually. After all channels in a slice receive the DPD command, the internal power circuit will enter off state IDD8.

Figure 40 — Deep Power Down

4.15.2 Deep Power Down Exit

For Deep Power Down exit, the RST_n micropillar is used.

Because RST_n is per slice (not per channel), all channels on that slice will exit Deep Power Down mode.

The Deep Power Down Exit sequence follows step 2 thru 5 in Power up and initialization sequence (sequence after power ramp).

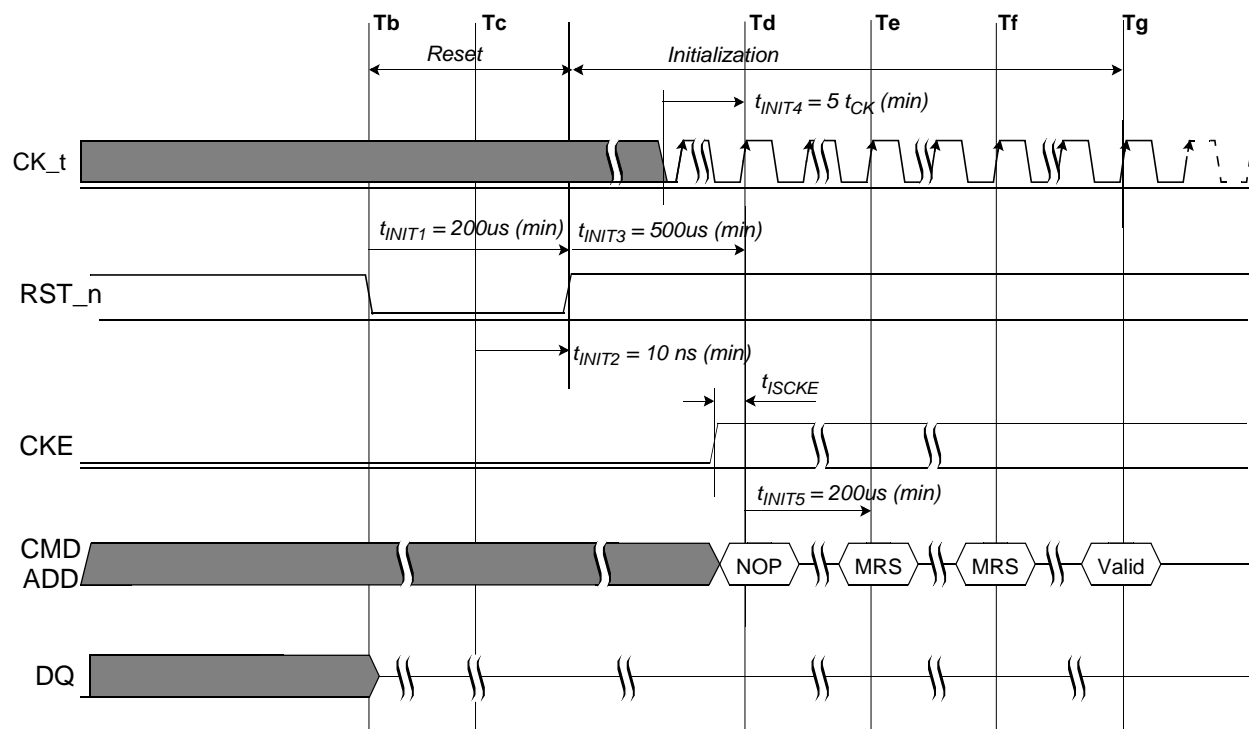


Figure 41 — Deep Power Down Exit

4.16 Input Clock Stop and Frequency Change

Wide I/O devices support input clock frequency change during CKE LOW under the following conditions:

- $t_{CK(MIN)}$ and $t_{CK(MAX)}$ are met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REF commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (t_{RCD} , t_{RP}) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{CH(abs)}$ and $t_{CL(abs)}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRS commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

4.16 Input Clock Stop and Frequency Change (cont'd)

Wide I/O devices support clock stop during CKE LOW under the following conditions:

- CK_t is held LOW (and CK_c is held HIGH if differential clock is supported) during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REF commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (t_{RCD} , t_{RP}) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies $t_{\text{CH(ABS)}}$ and $t_{\text{CL(ABS)}}$ for a minimum of 2 clock cycles prior to CKE going HIGH.

Wide I/O devices support input clock frequency change during CKE HIGH under the following conditions:

- $t_{\text{CK(MIN)}}$ and $t_{\text{CK(MAX)}}$ are met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- Any Activate, Read, Write, Precharge, Mode Register Set, or Status Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (t_{RCD} , t_{WR} , t_{RP} , t_{MRD} , t_{SRR} , etc.) have been met prior to changing the frequency;
- CS_n shall be held HIGH during clock frequency change;
- During clock frequency change, only REF commands may be executing;
- The Wide I/O device is ready for normal operation after the clock satisfies $t_{\text{CH(ABS)}}$ and $t_{\text{CL(ABS)}}$ for a minimum of $2t_{\text{CK}} + t_{\text{XP}}$.

After the input clock frequency is changed, additional MRS commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

Wide I/O devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW (and CK_c is held HIGH if differential clock is supported) during clock stop;
- CS_n shall be held HIGH during clock stop;
- Refresh Requirements apply during clock stop;
- During clock stop, only REF commands may be executing;
- Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
- The related timing conditions (t_{RCD} , t_{WR} , t_{RP} , t_{MRD} , t_{SRR} , etc.) have been met prior to stopping the clock;

The Wide I/O device is ready for normal operation after the clock is restarted and satisfies $t_{\text{CH(ABS)}}$ and $t_{\text{CL(ABS)}}$ for a minimum of $2t_{\text{CK}} + t_{\text{XP}}$.

4.17 No Operation Command

The purpose of the No Operation command (NOP) is to prevent the Wide I/O device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:

1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and RAS_n, CAS_n, WE_n HIGH at the clock rising edge N.

The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

4.18 Truth Table

Table 19 — Truth Table - Commands

NAME(FUNCTION)	CS#	RAS#	CAS#	WE#	BA	A10/ AP	A11/ SP	ADD	NOTES
DESELECT (NOP)	H	X	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	V	V	V	V	2
ACTIVATE (select bank and activate row)	L	L	H	H	BA	Row	Row	Row	
READ (select bank and column and start read burst), Full Preamble	L	H	L	H	BA	L	L	Col	
READ with AP (read burst with Auto Precharge), Full Preamble	L	H	L	H	BA	H	L	Col	3
READ (select bank and column and start read burst), Short Preamble	L	H	L	H	BA	L	H	Col	11
READ with AP (read burst with Auto Precharge), Short Preamble	L	H	L	H	BA	H	H	Col	3,11
WRITE (select bank and column and start write burst)	L	H	L	L	BA	L	V	Col	
WRITE with AP (write burst with Auto Precharge)	L	H	L	L	BA	H	V	Col	3
BURST TERMINATE or enter DEEP POWER DOWN	L	H	H	L	V	V	V	V	4,5
PRECHARGE (deactivate row in selected bank)	L	L	H	L	BA	L	V	V	6
PRECHARGE ALL (deactivate rows in all banks)	L	L	H	L	V	H	V	V	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	V	V	V	V	7,8,9
MODE REGISTER SET	L	L	L	L	BA	Op-code			10

V: H or L (defined logic level) X: either “defined or undefined (like floating) logic level.

NOTE 1 All states and sequences not shown are illegal or reserved.

NOTE 2 Deselect and NOP are functionally interchangeable.

NOTE 3 Autoprecharge is non-persistent. A10 High enables Auto Precharge, while A10 Low disables Autoprecharge

NOTE 4 Burst Terminate applies to only Read bursts or Write bursts with Auto Precharge disabled.

NOTE 5 This command is BURST TERMINATE if CKE is High and DEEP POWER DOWN entry if CKE is Low.

NOTE 6 If A10 is Low, bank address determines which bank is to be precharged. If A10 is High, all banks are precharged and BA0-BA1 are don't care.

NOTE 7 This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.

NOTE 8 All address inputs and I/O are ‘don't care’ except for CKE. Internal refresh counters control bank and row addressing.

NOTE 9 All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.

NOTE 10 A16, BA0 and BA1 values select the mode register.

NOTE 11 READ command with Short Preamble can only be used for zero bubble rank to rank, back to back Read cycles or Read interrupted by Read in the same rank. For details refer to chapter4.4.

NOTE 12 CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.

4.18 Truth Table (cont'd)**Table 20 — Truth Table - CKE and RST_n**

CKE N-1	CKE N	RST_n N-1	RST_n N	Current State	COMMAND N	ACTION N	NOTES
L	L	H	H	Power Down	X	Maintain Power Down	
L	L	H	H	Self Refresh	X	Maintain Self Refresh	
L	L	H	H	Deep Power Down	X	Maintain Deep Power Down	
L	H	H	H	Power Down	NOP or DESL	Exit Power Down	5,6,9
L	H	H	H	Self Refresh	NOP or DESL	Exit Self Refresh	5,7,10
L	L	H	L	Deep Power Down	X	Exit Deep Power Down	8
H	L	H	H	All banks Idle	NOP or DESL	Precharge Power Down Entry	5
H	L	H	H	Bank(s) Active	NOP or DESL	Active Power Down Entry	5
H	L	H	H	All Banks Idle	REFRESH	Self Refresh Entry	
H	L	H	H	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	H	H	See the other Truth Tables			

NOTE 1 CKE N is the logic state of CKE at clock edge N; CKE N-1 is the state of CKE at the previous clock edge.

RST_n is the logic state of RST_n N at clock edge n; RST_n N-1 is the state of RST_n N at the previous clock edge.

NOTE 2 Current state is the state of Wide I/O DRAM immediately prior to clock edge N.

NOTE 3 Command is the command registered at clock edge N, and ACTION N is the result of COMMAND N.

NOTE 4 All states and sequences not shown are illegal or reserved.

NOTE 5 DESELECT and NOP are functionally interchangeable.

NOTE 6 Power Down exit time (tXP) should elapse before a command other than NOP or DESELECT is issued.

NOTE 7 SELF REFRESH exit time (tXSR) should elapse before a command other than NOP or DESELECT is issued.

NOTE 8 The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.

NOTE 9 The clock must toggle at least once during the tXP period.

NOTE 10 The clock must toggle at least once during the tXSR time.

Table 21 — Truth table - Current state Bank n -Command to Bank n

Current State	Command	Operation	Next State	NOTES
Any	NOP, DESL	Continue Previous operation	Current state	
Idle	ACTIVATE	Select and activate row	Active	
	AUTO REFRESH	Begin to refresh	Refresh	6
	MODE REGISTER SET	Load value to Mode Register	MR Write	6
	PRECHARGE	Deactivate row in bank or banks	Precharge	7,14
Active	READ	Select column, and start read burst	Read	9
	WRITE	Select column, and start write burst	Write	10
	PRECHARGE	Deactivate row in bank or banks	Precharge	7
Read (Auto Precharge disabled)	READ	Select column, and start new read burst	Read	8,9
	WRITE	Select column, and start write burst	Write	8,10,11
	BST	Read burst terminate	Active	12
Write (Auto Precharge Disabled)	READ	Select column, and start read burst	Read	8,9,13
	WRITE	Select column, and start new write burst	Write	8,11
	BST	Write burst terminate	Active	12

4.18 Truth Table (cont'd)

Notes to Table 21

NOTE 1 The table applies when both CKE N-1 and CKE N are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current state definitions

Idle: The bank or banks have been precharged, and tRP has been met.

Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.

Reading: A Read burst has been initiated with Auto Precharge disabled and has not yet terminated or been terminated.

Writing: A Write burst has been initiated with Auto Precharge disabled and has not yet terminated or been terminated.

NOTE 4 The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state.

Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the Active state

Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.

Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

NOTE 5 The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.

Refreshing: starts with registration of an Auto Refresh command and ends when tRFC is met. Once tRFC is met, the device will be in an all banks idle state.

MR writing: starts with the registration of a MRS command and ends when tMRD has been met. Once tMRD has been met, the bank will be in the Idle state.

Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

NOTE 6 Not bank-specific; requires that all banks are idle and no bursts are in progress.

NOTE 7 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

NOTE 8 A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.

NOTE 9 Reads listed in the Command column can be Reads w/ Auto Precharge enabled or Reads w/ Auto Precharge disabled. Also they can be Reads Full Preamble or Reads Short Preamble. Reads with Short Preamble can only be used for zero bubble rank to rank, back to back Read cycles, or Read interrupt by Read in the same rank. For details refer to 4.2.

NOTE 10 Writes listed in the command column can be Writes w/ Auto Precharge enabled or Writes w/ Auto Precharge disabled.

NOTE 11 A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.

NOTE 12 Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank.

NOTE 13 A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.

NOTE 14 If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

4.18 Truth Table (cont'd)**Table 22 — Truth table - Current State Bank n -Command to Bank m**

Current State	Command	Operation	Next State	NOTES
Any	NOP,DESL	Continue Previous operation	Current state of Bank m	
Idle	Any	Any command allowed to Bank m	-	14
Row Activating ,Active,or Precharge	ACTIVATE	Select and activate row in bank m	Active	7
	READ	Select column, and start read burst from bank m	Read	8
	WRITE	Select column, and start write burst to bank m	Write	9
	PRECHARGE	Deactivate row in bank or banks	Precharge	10
	BST	Read or write burst terminate an ongoing Read/Write from/to bank m	Active	14
Read (Auto Precharge Disabled)	READ	Select column, and start read burst from Bank m	Read	8
	WRITE	Select column, and start write burst to Bank m	Write	9,11
	ACTIVATE	Select and activate row in Bank m	Active	
	PRECHARGE	Deactivate row in bank or banks	Precharge	10
Write (Auto Precharge Disabled)	READ	Select column, and start read burst from Bank m	Read	8,13
	WRITE	Select column, and start write burst to Bank m	Write	9
	ACTIVATE	Select and activate row in Bank m	Active	
	PRECHARGE	Deactivate row in bank or banks	Precharge	10
Read with Autoprecharge	READ	Select column, and start read burst from Bank m	Read	8,12
	WRITE	Select column, and start write burst to Bank m	Write	9,11,12
	ACTIVATE	Select and activate row in Bank m	Active	
	PRECHARGE	Deactivate row in bank or banks	Precharge	10
Write with Autoprecharge	READ	Select column, and start read burst from Bank m	Read	8,12,13
	WRITE	Select column, and start write burst to Bank m	Write	9,12
	ACTIVATE	Select and activate row in Bank m	Active	
	PRECHARGE	Deactivate row in bank or banks	Precharge	10

NOTE 1 The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.

NOTE 2 All states and sequences not shown are illegal or reserved.

NOTE 3 Current State Definitions:

Idle: the bank has been precharged, and tRP has been met.

Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

Read: a Read burst has been initiated with Auto Precharge disabled and has not yet terminated or been terminated.

Write: a Write burst has been initiated with Auto Precharge disabled and has not yet terminated or been terminated.

NOTE 4 Refresh, Self-Refresh, and Mode Register Set commands may only be issued when all bank are idle.

NOTE 5 A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.

NOTE 6 The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:

MR Writing: starts with the registration of a MRS command and ends when tMRD has been met. Once tMRD has been met, the bank will be in the Idle state.

NOTE 7 tRRD must be met between an Activate command to Bank n and a subsequent Activate command to Bank m.

NOTE 8 Reads listed in the Command column can be Reads w/ Auto Precharge enabled or Reads w/ Auto Precharge disabled. Also they can be Reads Full Preamble or Reads Short Preamble. Reads with Short Preamble can only be used for zero bubble rank to rank, back to back Read cycles, or Read interrupt by Read in the same rank. For details refer to 4.2.

NOTE 9 Writes listed in the command column can be Writes w/ Auto Precharge enabled or Writes w/ Auto Precharge disabled.

NOTE 10 This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

4.18 Truth Table (cont'd)

Notes to Table 22 (cont'd)

NOTE 11 A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to asserting a Write command.

NOTE 12 Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions in Table 42.

NOTE 13 A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.

NOTE 14 BST is allowed only if a Read or Write burst is ongoing.

5 Boundry Scan

5.1 Implementation

Capture signal state, then scan out.

Output Mux can set DQ to a known state from scan chain.

- Complements scan capture capability

Global scan enable

- SSEN micropillar on lower right NC, opposite diagonal from KEY

CA and DQ Rx active only on parallel input mode are necessary.

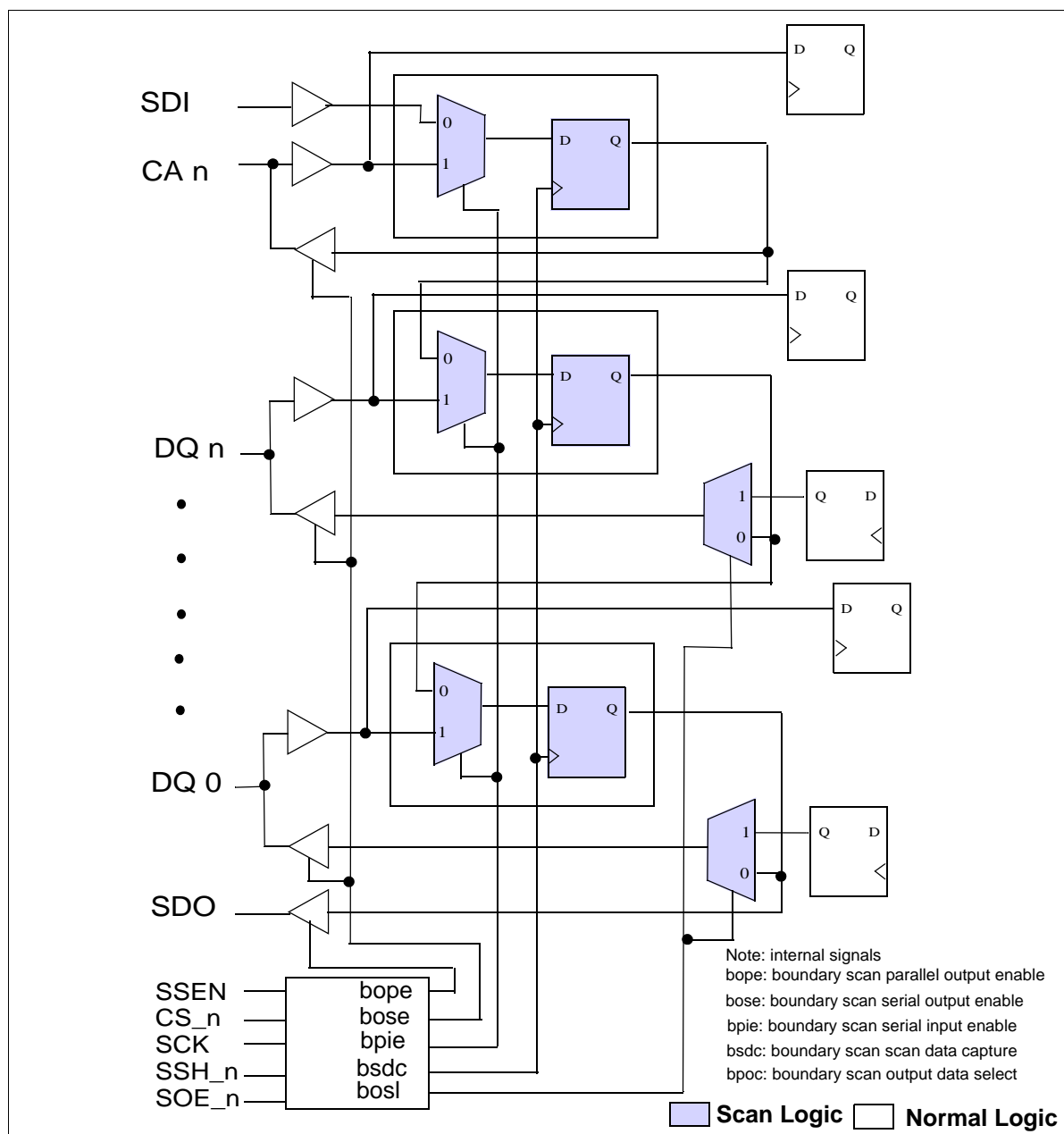


Figure 42 — Conceptual Block diagram

5.2 Scan Chain Order

- Chain starts near the middle of the die and works out from there.
- The exit order is the reverse of this, so A0 is the first bit to exit the chain and DQ112 is the last.
- The following signals are excluded: Power, NC, DA, DA(o), TEST, CS_n, SSN, SSH_n, SDI, SCK, SDO, SOE_n, RST_n, and VPIN.
- A12 thru A15 will be included in boundary scan chain regardless of memory density. Scan Chain order

Table 23 — Boundary scan exit order (per channel)

BIT #	Location	Signal name	BIT #	Location	Signal name	BIT #	Location	Signal name	BIT#	Location	Signal name	BIT#	Location	Signal name
1	A2	A0	41	B13	DQ11	81	C24	DQ44	121	E34	DQ78	161	F45	DQ127
2	B2	A1	42	A13	DM1	82	D24	DQ45	122	F34	DQ79	162	E45	DQ126
3	C2	A2	43	C14	DQ12	83	E24	DQ46	123	F35	DQ95	163	D45	DQ125
4	D2	A3	44	D14	DQ13	84	F24	DQ47	124	E35	DQ94	164	C45	DQ124
5	E2	A4	45	E14	DQ14	85	F25	DQ63	125	D35	DQ93	165	A46	DM15
6	F2	A5	46	F14	DQ15	86	E25	DQ62	126	C35	DQ92	166	B46	DQ123
7	F3	A6	47	F15	DQ31	87	D25	DQ61	127	A36	DM11	167	E46	DQ122
8	E3	A7	48	E15	DQ30	88	C25	DQ60	128	B36	DQ91	168	F46	DQ121
9	D3	A8	49	D15	DQ29	89	A26	DM7	129	E36	DQ90	169	F47	DQ120
10	C3	A9	50	C15	DQ28	90	B26	DQ59	130	F36	DQ89	170	E47	DQ119
11	C4	A10	51	A16	DM3	91	E26	DQ58	131	F37	DQ88	171	D47	DQS7_t
12	D4	A11	52	B16	DQ27	92	F26	DQ57	132	E37	DQ87	172	A48	DM14
13	E4	A12	53	E16	DQ26	93	F27	DQ56	133	D37	DQS5_t	173	B48	DQ118
14	F4	A13	54	F16	DQ25	94	E27	DQ55	134	A38	DM10	174	E48	DQ117
15	F5	A14	55	F17	DQ24	95	D27	DQS3_t	135	B38	DQ86	175	F48	DQ116
16	E5	A15	56	E17	DQ23	96	A28	DM6	136	E38	DQ85	176	F49	DQ115
17	D5	BA0	57	D17	DQS1_t	97	B28	DQ54	137	F38	DQ84	177	E49	DQ114
18	C5	BA1	58	A18	DM2	98	E28	DQ53	138	F39	DQ83	178	D49	DQ113
19	A6	CK_t	59	B18	DQ22	99	F28	DQ52	139	E39	DQ82	179	C49	DQ112
20	C6	RAS_n	60	E18	DQ21	100	F29	DQ51	140	D39	DQ81			
21	D6	CAS_n	61	F18	DQ20	101	E29	DQ50	141	C39	DQ80			
22	E6	WE_n	62	F19	DQ19	102	D29	DQ49	142	C40	DQ96			
23	F6	A16	63	E19	DQ18	103	C29	DQ48	143	D40	DQ97			
24	F7	CKE1	64	D19	DQ17	104	C30	DQ64	144	E40	DQ98			
25	E7	CKE0	65	C19	DQ16	105	D30	DQ65	145	F40	DQ99			
26	E8	CKE3	66	C20	DQ32	106	E30	DQ66	146	F41	DQ100			
27	F8	CKE2	67	D20	DQ33	107	F30	DQ67	147	E41	DQ101			
28	C10	DQ0	68	E20	DQ34	108	F31	DQ68	148	B41	DQ102			
29	D10	DQ1	69	F20	DQ35	109	E31	DQ69	149	A41	DM12			
30	E10	DQ2	70	F21	DQ36	110	B31	DQ70	150	D42	DQS6_t			
31	F10	DQ3	71	E21	DQ37	111	A31	DM8	151	E42	DQ103			
32	F11	DQ4	72	B21	DQ38	112	D32	DQS4_t	152	F42	DQ104			
33	E11	DQ5	73	A21	DM4	113	E32	DQ71	153	F43	DQ105			
34	B11	DQ6	74	D22	DQS2_t	114	F32	DQ72	154	E43	DQ106			
35	A11	DM0	75	E22	DQ39	115	F33	DQ73	155	B43	DQ107			
36	D12	DQS0_t	76	F22	DQ40	116	E33	DQ74	156	A43	DM13			
37	E12	DQ7	77	F23	DQ41	117	B33	DQ75	157	C44	DQ108			
38	F12	DQ8	78	E23	DQ42	118	A33	DM9	158	D44	DQ109			
39	F13	DQ9	79	B23	DQ43	119	C34	DQ76	159	E44	DQ110			
40	E13	DQ10	80	A23	DM5	120	D34	DQ77	160	F44	DQ111			

5.2 Scan Chain order (cont'd)

50	VSS	VSS				
49	VSS	VSS	DQ112	DQ113	DQ114	DQ115
48	DM14	DQ118	VSSQ	VSSQ	DQ117	DQ116
47			DQS7_n	DQS7_t	DQ119	DQ120
46	DM15	DQ123	VDDQ	VDDQ	DQ122	DQ121
45			DQ124	DQ125	DQ126	DQ127
44			DQ108	DQ109	DQ110	DQ111
43	DM13	DQ107	VDDQ	VDDQ	DQ106	DQ105
42			DQS6_n	DQS6_t	DQ103	DQ104
41	DM12	DQ102	VSSQ	VSSQ	DQ101	DQ100
40	VSS	VSS	DQ96	DQ97	DQ98	DQ99
39	VSS	VSS	DQ80	DQ81	DQ82	DQ83
38	DM10	DQ86	VSSQ	VSSQ	DQ85	DQ84
37			DQS5_n	DQS5_t	DQ87	DQ88
36	DM11	DQ91	VDDQ	VDDQ	DQ90	DQ89
35			DQ92	DQ93	DQ94	DQ95
34			DQ76	DQ77	DQ78	DQ79
33	DM9	DQ75	VDDQ	VDDQ	DQ74	DQ73
32			DQS4_n	DQS4_t	DQ71	DQ72
31	DM8	DQ70	VSSQ	VSSQ	DQ69	DQ68
30	VSS	VSS	DQ64	DQ65	DQ66	DQ67
29	VSS	VSS	DQ48	DQ49	DQ50	DQ51
28	DM6	DQ54	VSSQ	VSSQ	DQ53	DQ52
27			DQS3_n	DQS3_t	DQ55	DQ56
26	DM7	DQ59	VDDQ	VDDQ	DQ58	DQ57
25			DQ60	DQ61	DQ62	DQ63
24			DQ44	DQ45	DQ46	DQ47
23	DM5	DQ43	VDDQ	VDDQ	DQ42	DQ41
22			DQS2_n	DQS2_t	DQ39	DQ40
21	DM4	DQ38	VSSQ	VSSQ	DQ37	DQ36
20	VSS	VSS	DQ32	DQ33	DQ34	DQ35
19	VSS	VSS	DQ16	DQ17	DQ18	DQ19
18	DM2	DQ22	VSSQ	VSSQ	DQ21	DQ20
17			DQS1_n	DQS1_t	DQ23	DQ24
16	DM3	DQ27	VDDQ	VDDQ	DQ26	DQ25
15			DQ28	DQ29	DQ30	DQ31
14			DQ12	DQ13	DQ14	DQ15
13	DM1	DQ11	VDDQ	VDDQ	DQ10	DQ9
12			DQS0_n	DQS0_t	DQ7	DQ8
11	DM0	DQ6	VSSQ	VSSQ	DQ5	DQ4
10	VSS	VSS	DQ0	DQ1	DQ2	DQ3
9	VSS	VSS				
8			CS3_n	CS2_n	CKE3	CKE2
7			CS0_n	CS1_n	CKE0	CKE1
6	CK_t		RAS_n	CAS_n	WE_n	A16
5	VSS	VSS	BA1	BA0	A15	A14
4			A10	A11	A12	A13
3			A9	A8	A7	A6
2	A0	A1	A2	A3	A4	A5
1	VSS	VSS	(Note 1)			
	A	B	C	D	E	F

NOTE 1 This is Key (missing micropillar) for channel d, NC for channel b, VPIN for channel A, and SSEN for channel c

NOTE 2 Channel descriptors are not explicitly shown. For details refer to micropillar Definition and Description.

Figure 43 — Scan chain order (per channel)

5.2 Scan Chain order (cont'd)

Table 24 — Scan Micropillar description

Location	Symbol	Type	Description
E9	SSH_n[a:d]	Input	Scan Shift: capture the data input from the micropillar at logic HIGH and shift the data on the chain at logic LOW.
C9	SCK[a:d]	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to the rising edge of the scan clock.
D9	SDI[a:d]	Input	Serial Data Input
B8	SDO[a:d]	Output	Serial Data Output
C1, Chc	SSEN	Input	Scan Enable: logic HIGH enables scan logic. Scan logic is disabled at logic LOW. Must be tied to VSS or VSSQ when not in use.
F8	SOE_n[a:d]	Input	Scan Output Enable: enables (registered LOW) and disables (registered HIGH) DQ Tx or SDO

Table 25 — Boundary Scan Truth Table

Description	SSEN	CS_n	SOE_n	SSH_n	SDI	SDO	DQ, CA	SCK
Serial Data In/out	H	L	L	L	Valid	Valid	HiZ	Valid CLK
Serial data In (No Serial out)	H	L	H	L	Valid	HiZ	HiZ	Valid CLK
Parallel Input	H	H	H	H	x	HiZ	Valid Data In	Valid CLK
Parallel Output	H	L	H	H	x	HiZ	Valid Data Out	x
NOP (DQ,SDO both float, no data capture)	H	H	x	L	x	HiZ	HiZ	x
Normal DRAM functionality, Scan chain disabled	L	Valid	x	x	x	HiZ		x

NOTE Channel descriptors are not explicitly shown for signal name.

x: Don't care (VIH or VIL)

Table 26 — Boundary Scan AC characteristics

Parameter	Symbol	Min	Max	Unit
Clock cycle time	tSCK	40	-	ns
Scan enable setup time	tSES	20	-	ns
Scan enable hold time	tSEH	20	-	ns
Scan command setup time for CS_n, SOE_n, SSH_n	tSCS	14	-	ns
Scan command hold time for CS_n, SOE_n, SSH_n	tSCH	14	-	ns
Scan capture setup time	tSDS	10	-	ns
Scan capture hold time	tSDH	10	-	ns
Valid scan output	tSAC	-	10	ns
Scan output hold	tSOH	1.0	-	ns
Scan output Low Z	tSLZ	1.0	-	ns
Scan output Hi Z	tSHZ	-	10	ns

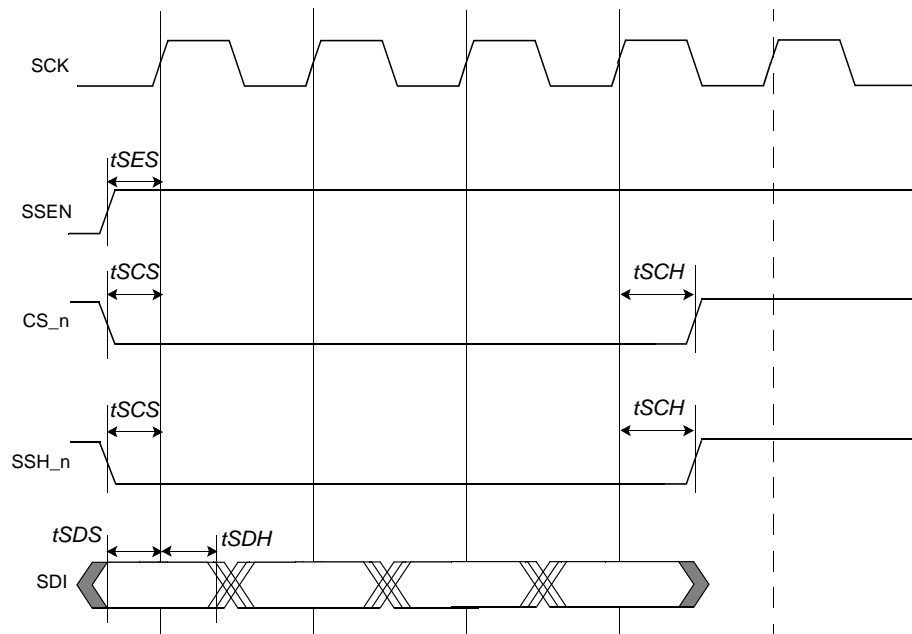


Figure 44 — Serial Data In (synchronous operation)

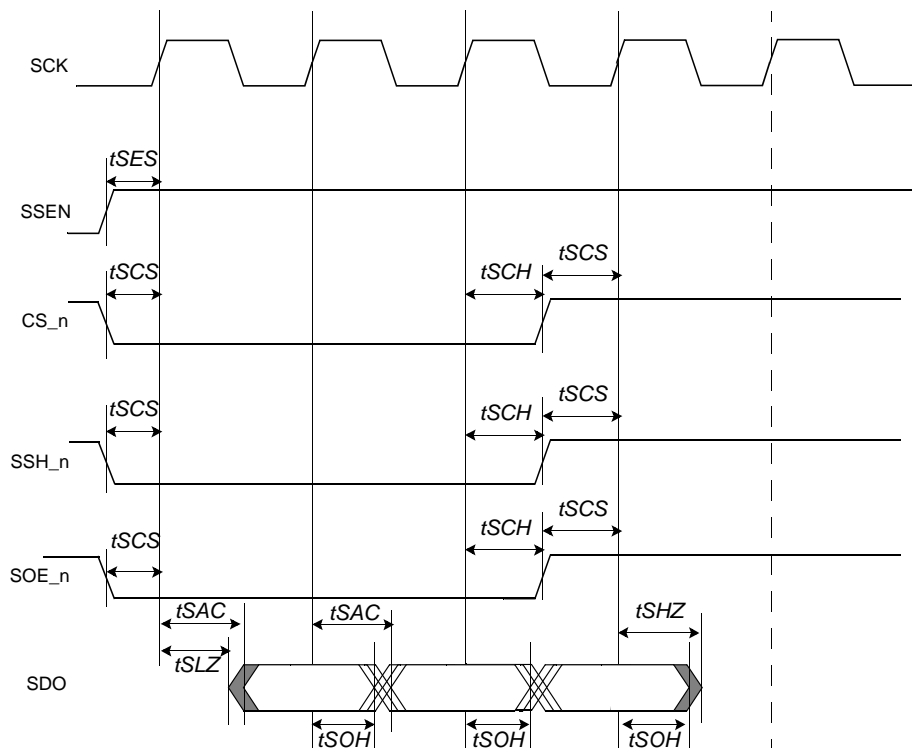


Figure 45 — Serial Data Out (synchronous operation)

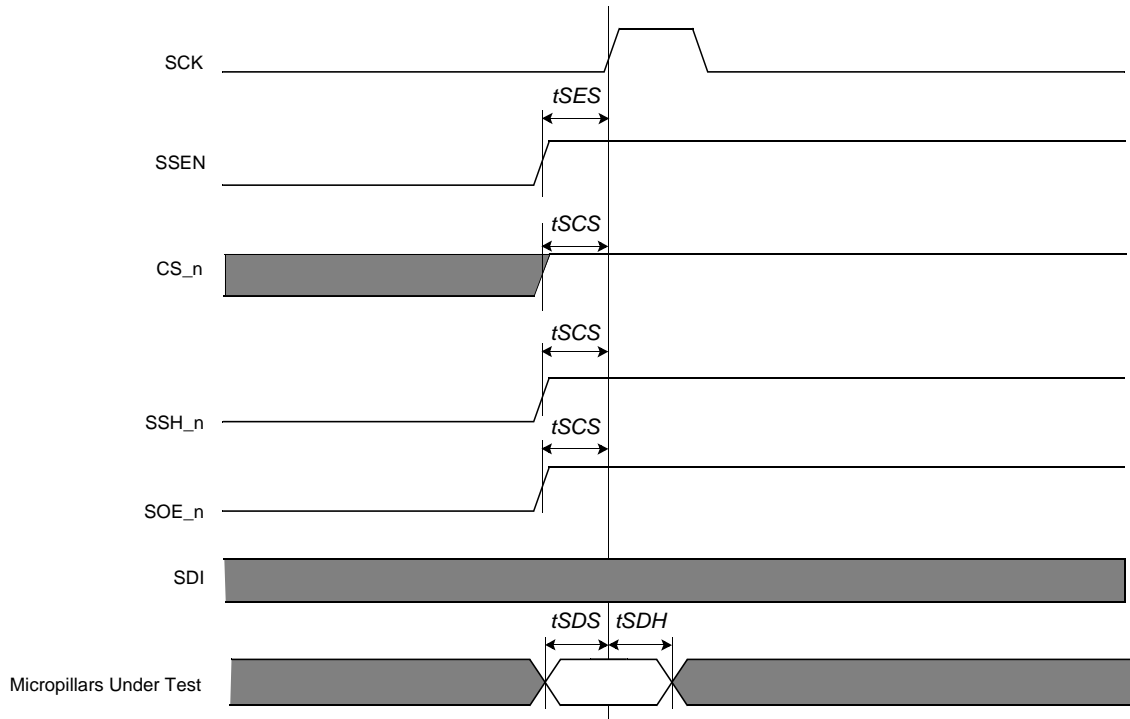


Figure 46 — Parallel Data In (synchronous operation)

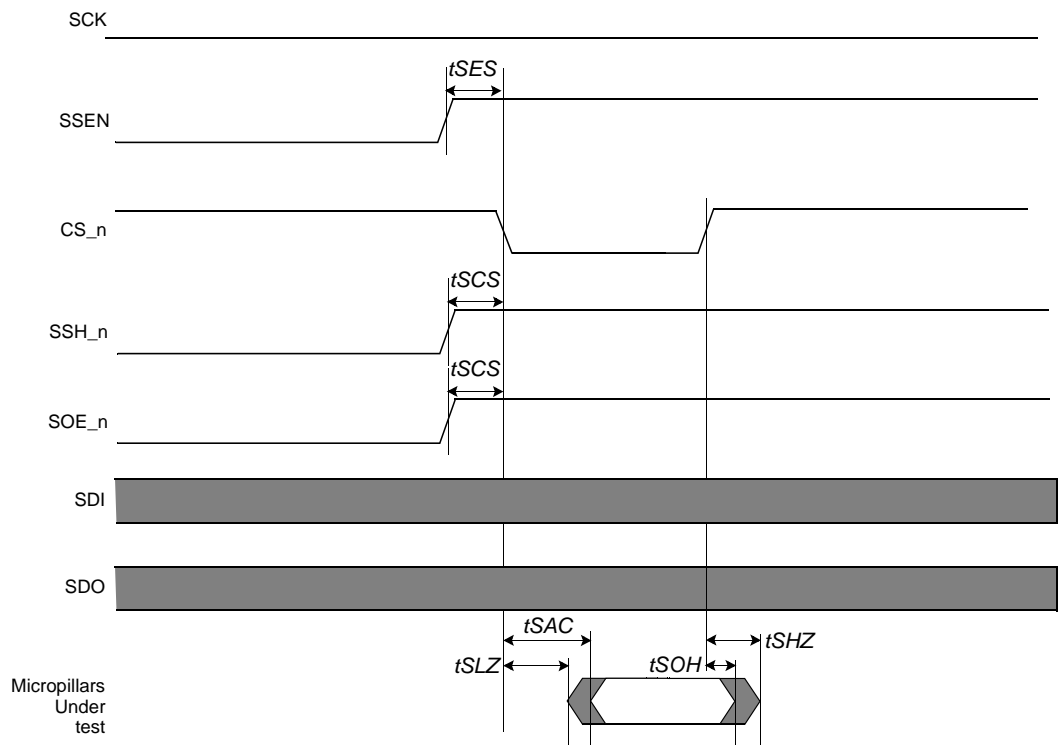


Figure 47 — Parallel Out (asynchronous operation)

6 Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 27 — Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2
Voltage on any I/O micropillar relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	T _{STG}	-55	125	C	3

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NOTE 2 See 3.2.2, Power-Ramp, for relationships between power supplies.

NOTE 3 Storage Temperature is the die surface temperature on the center/top side of the Wide I/O chip. For the measurement conditions, please refer to the JEDEC standard.

7 AC and DC Operating Conditions

7.1 Recommended DC Operating Conditions

Table 28 — DC Operating Conditions

Symbol	Wide I/O			DRAM	Unit
	Min	Typ	Max		
VDD1	1.70	1.80	1.95	Core Power1	V
VDD2	1.14	1.20	1.3	Core Power2 and Control/Address Input Buffer Power	V
VDDQ	1.14	1.20	1.3	I/O Buffer Power	V

NOTE 1 VDD1 uses significantly less power than VDD2

NOTE 2 The voltage range for VDD1, VDD2 and VDDQ is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 1MHz at the DRAM micropillar.

7.2 Input Leakage Current

Table 29 — Input Leakage Current

Parameter / Condition	Symbol	Min	Max	Unit
Input Leakage current (0 ≤ VIN ≤ VDD2(orVDDQ))	IL	-5	5	uA

7.3 Operating Temperature Range

Table 30 — Operating Temperature Range

Parameter / Condition	Symbol	Min	Max	Unit
Standard	Toper	-25	85	C
High		85	105	C

NOTE 1 Operating Temperature is the backside temperature of center of Wide I/O DRAM device

NOTE 2 Some applications require operating the Wide I/O DRAM in the maximum temperature conditions of the High

Temperature Range between 85 °C and 105 °C case temperature. For Wide I/O DRAM devices, some derating is necessary to operate in this range. See 3.3.3.1, Status Register Read.

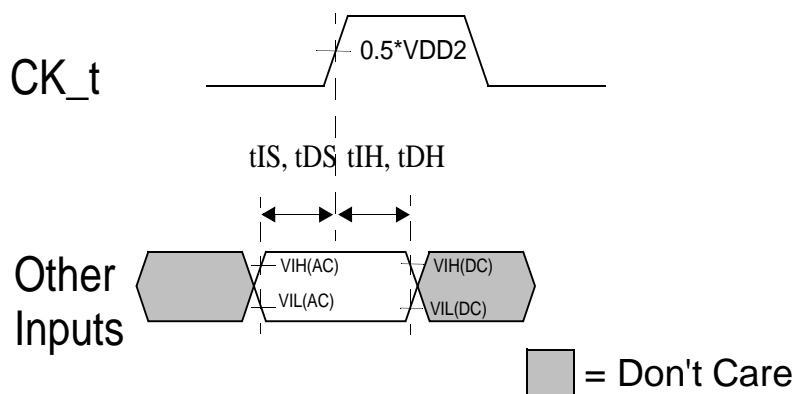
NOTE 3 Either the device case temperature or the temperature sensor (See 3.3.3.1, Status register read) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature.

7.4 AC and DC Input Measurement Levels

Table 31 — AC and DC Input Measurement Levels

Parameter	Symbol	Min	Max	Unit
Input high level (AC)	VIH(AC)	$0.80 \cdot VDD2(\text{or } VDDQ)$	$VDD2(\text{or } VDDQ) + 0.2$	V
Input low level (AC)	VIL(AC)	-0.2	$0.20 \cdot VDD2(\text{or } VDDQ)$	V
Input high level (DC)	VIH(DC)	$0.70 \cdot VDD2(\text{or } VDDQ)$	$VDD2(\text{or } VDDQ) + 0.2$	V
Input low level (DC)	VIL(DC)	-0.2	$0.30 \cdot VDD2(\text{or } VDDQ)$	V

NOTE 1 VDD2 for ADD/CMD micropillars, VDDQ for DQ/DM/DQS micropillars.



Note:

AC timing is defined with 1V/ns input slew rate on CK.

AC level is guaranteed transition point.

DC level is hysteresis.

Figure 48 — Input AC timing definition

8 AC and DC Output Meassurement Levels

8.1 Output Levels

Table 32 — Output Levels

Parameter	Symbol	Min	Max	Unit
Output high voltage	VOH	0.80 * VDDQ	-	V
Output low voltage	VOL	-	0.20 * VDDQ	V

NOTE 1 Output timing reference voltage is VOH/VOL for DQ, 0.5*VDDQ for DQS.

NOTE 2 Output AC timing is defined with 1V/ns output slew rate on CK/DQS.

NOTE 3 Output slew rate is defined between VOH and VOL.

8.2 Output Timing Reference Load

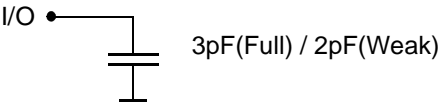


Figure 49 — Timing reference load

8.3 Output Slew Rate

With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between VOL and VOH for single ended signals

Table 33 — Output Slew Rate

Description	Measured		Defined by
	from	to	
Output slew rate for rising edges	VOL	VOH	(VOH-VOL) / Tr
Output slew rate for falling edges	VOH	VOL	(VOH-VOL) / Tf

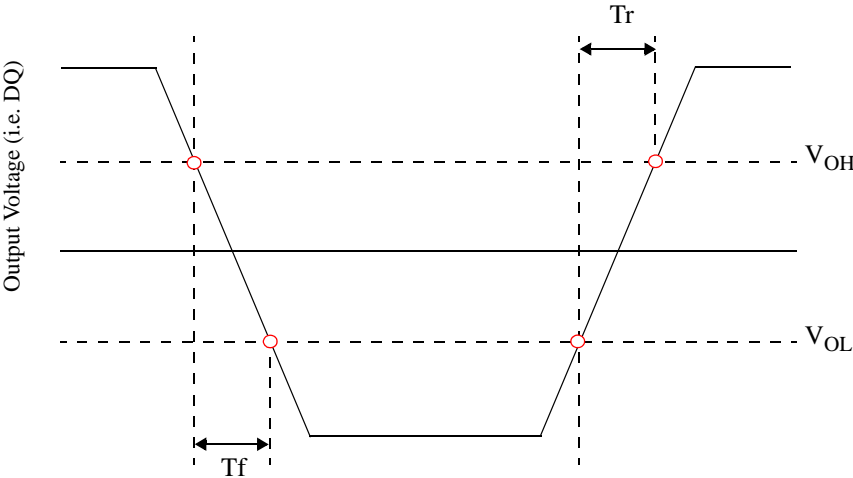


Figure 50 — Output Slew Rate Definition

Table 34 — Output Slew Rate

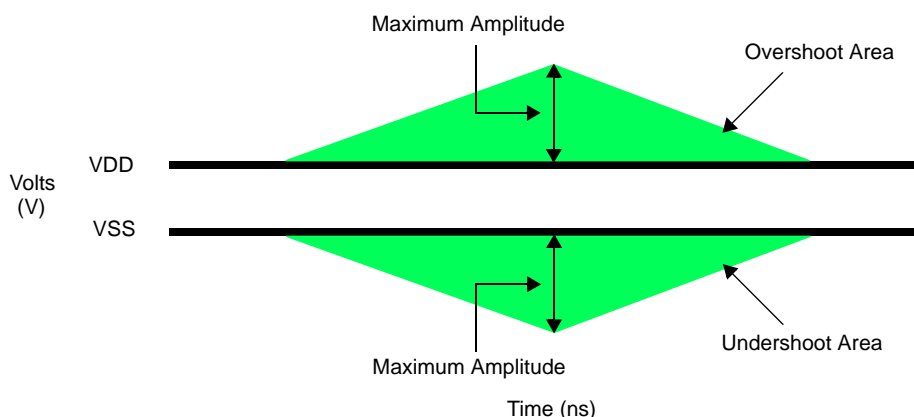
Parameter	Symbol	Min	Max	Unit
Output Slew rate	SRQ	1.0	-	V/ns

NOTE 1 Full strength driver for 3pF load condition, weak strength driver for 2pF load condition

8.4 Over/Undershoot

Table 35 — Over/Undershoot

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.35V
Maximum peak Amplitude allowed for undershoot area	0.35V
Maximum overshoot area above VDD2/VDDQ	0.8V-ns
Maximum undershoot area below VSS/VSSQ	0.8V-ns



NOTE 1 For CKE, CK, Address and CMD, VDD stands for VDD2. For DQ and DMQS, VDD stands for VDDQ.

NOTE 2 For CKE, CK, Address and CMD, VSS stands for VSS. For DQ and DMQS, VSS stands for VSSQ.

Figure 51 — AC Overshoot and Undershoot Definition for Address and Control Micropillars

9 Input/Output Capacitance

Table 36 — Input/Output Capacitance

Parameter	Symbol	Min	Max	Unit
Input capacitance, RST_n	Cin_RST_n	-	1.0	pF
Input capacitance, all other input-only micropillars	Cin	-	0.5	pF
Input/output capacitance, DQ/DM/DQS	Cio	-	0.5	pF

NOTE 1 These capacitance values are for single monolithic devices only. Multiple die stacks will have parallel capacitive loads.

NOTE 2 micropillars for test purposes (TEST, DA, VPIN, and Boundary Scan micropillars) do not comply with above table.

10 IDD Specification Parameters and Test Conditions

10.1 IDD Measurement Conditions

The following definitions and conditions are used in the IDD measurement tables unless stated otherwise:

- a) LOW: VIN - VIL(DC)max
- b) HIGH: VIN - VIH(DC)min
- c) STABLE: Inputs are stable at a HIGH or LOW level
- d) SWITCHING: See Table 2 through Table 5

Table 37 — SDR Switching for Command and Address Input Signals, IDD2P, IDD2N, IDD3P, IDD3N

	CK (Rising)	CK (Rising)	CK (Rising)	CK (Rising)	CK (Rising)	CK (Rising)	CK (Rising)	CK (Rising)
Cycle	0	1	2	3	4	5	6	7
CS _n	HIGH							
RAS _n	H	L	L	H	H	L	L	H
CAS _n	L	L	H	H	L	L	H	H
WE _n	H	L	L	H	H	L	L	H
A0	L	L	H	H	L	L	H	H
A1	H	L	L	H	H	L	L	H
A2	L	L	H	H	L	L	H	H
A3	H	L	L	H	H	L	L	H
A4	L	L	H	H	L	L	H	H
A5	H	L	L	H	H	L	L	H
A6	L	L	H	H	L	L	H	H
A7	H	L	L	H	H	L	L	H
A8	L	L	H	H	L	L	H	H
A9	H	L	L	H	H	L	L	H
A10	L	L	H	H	L	L	H	H
A11	H	L	L	H	H	L	L	H
A12	L	L	H	H	L	L	H	H
A13	H	L	L	H	H	L	L	H
A14	L	L	H	H	L	L	H	H
A15	H	L	L	H	H	L	L	H

NOTE 1 CS_n must always be driven HIGH.

NOTE 2 For each clock cycle, 50% of the address bus is changing between HIGH and LOW.

The noted pattern (N, N + 1, N + 2, N + 3...) is used continuously during I_{DD} measurement for I_{DD} values that require switching on the address bus.

10.1 IDD Measurement Conditions (cont'd)

Table 38 — SDR Switching for I_{DD0}

Loop	Clock Cycle Number	Clock	CK E	CS_ n	Command	RAS_n CAS_n WE_n	BA[1:0]	Address	DQ
0	0	Rising	H	L	ACTIVE	LHH	00	LHLHLHLHLHLHLHLH	L
0	1	Rising	H	H	DESELECT	LHL	00	LLLLLLLLLLLLLLLLL	
0	2	Rising	H	L	NOP	HHH	00	HLHLHLHLHLHLHLHL	
0	3	Rising	H	H	DESELECT	HLL	00	HHHHHHHHHHHHHHHHH	
0	4	Rising	H	L	NOP	HHH	00	LHLHLHLHLHLHLHLH	
0	5	Rising	H	H	DESELECT	LHH	00	LLLLLLLLLLLLLLLLL	
0	6	Rising	H	L	NOP	HHH	00	HLHLHLHLHLHLHLHL	
0	7	Rising	H	H	DESELECT	HLL	00	HHHHHHHHHHHHHHHHH	
0	8	Rising	H	L	PRE-CHARGE	HLH	00	LHLHLHLHLHLHLHLH	
0	9	Rising	H	H	DESELECT	LHH	00	LLLLLLLLLLLLLLLLL	
0	10	Rising	H	L	NOP	HHH	00	HLHLHLHLHLHLHLHL	
0	11	Rising	H	H	DESELECT	HLH	00	HHHHHHHHHHHHHHHHH	
1	12 - 23	Repeat Loop 0 with BA[1:0] = 01							
2	24 - 35	Repeat Loop 0 with BA[1:0] = 10							
3	36 - 47	Repeat Loop 0 with BA[1:0] = 11							
4		Repeat Loops 0-3							

Table 39 — SDR Switching for I_{DD4R}

Loop	Clock Cycle Number	Clock	CK E	CS _n	Command	RAS _n CAS _n WE _n	BA[1:0]	Address	DQ (per byte)
0	0	Rising	H	L	READ	HLH	00	LHLHLHLHLHLHLHLH	0x33
0	1	Rising	H	H	DESELECT	LHL	00	LLLLLLLLLLLLLLLLL	0xF0
0	2	Rising	H	H	DESELECT	LHL	00	HLHLHLHLHLHLHLH	0x3C
0	3	Rising	H	H	DESELECT	HLH	00	HHHHHHHHHHHHHHHHH	0x0F
1	4 - 7	Repeat Loop 0 with BA[1:0] = 01							
2	8 - 11	Repeat Loop 0 with BA[1:0] = 10							
3	12 - 15	Repeat Loop 0 with BA[1:0] = 11							
4		Repeat Loops 0-3							

NOTE 1 DQ, DQS_t, DQS_c are at mid-level when not driving data in burst sequence.

NOTE 2 DM is LOW.

NOTE 3 All banks will remain open during data burst loops.

NOTE 4 DQ switching 50% on each burst data transfer.

10.1 IDD Measurement Conditions (cont'd)**Table 40 — SDR Switching for I_{DD4W}**

Loop	Clock Cycle Number	Clock	CK E	CS _n	Command	RAS _n CAS _n WE _n	BA[1:0]	Address	DQ (per byte)
0	0	Rising	H	L	WRITE	HLL	00	LHLHLHLHLHLHLHLH	0x33
0	1	Rising	H	H	DESELECT	LHH	00	LLLLLLLLLLLLLLLLL	0xF0
0	2	Rising	H	H	DESELECT	LHH	00	HLHLHLHLHLHLHLH	0x3C
0	3	Rising	H	H	DESELECT	HLL	00	HHHHHHHHHHHHHHHHH	0x0F
1	4 - 7	Repeat Loop 0 with BA[1:0] = 01							
2	8 - 11	Repeat Loop 0 with BA[1:0] = 10							
3	12 - 15	Repeat Loop 0 with BA[1:0] = 11							
4		Repeat Loops 0-3							

NOTE 1 Data mask (DM) must always be driven LOW (data NOT masked).

NOTE 2 All banks remain open during data burst loops.

NOTE 3 DQ switching 50% on each burst data transfer.

10.2 IDD Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entire standard temperature range, with the exception of I_{DD6ET} which is for the elevated temperature range. All specifications apply to the device on a per-die basis, with a single channel in the required state for the applicable measurement parameter, and all other channels in the Idle Power-Down Standby state.

Table 41 — I_{DD} Specification Parameters and Operating ConditionsNotes 1, 2 & 3 apply for all values. CA bus is comprised of RAS_n, CAS_n, WE_n, and A[msb:lsb].

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: t _{CK} = t _{CKmin} ; t _{RC} = t _{RCmin} ; CKE is HIGH; CS _n is HIGH between valid commands; CA bus inputs are switching; Data bus inputs are stable	I _{DD01}	V _{DD1}	
	I _{DD02}	V _{DD2}	
	I _{DD0in}	V _{DDQ}	
Idle power-down standby current: t _{CK} = t _{CKmin} ; CKE is LOW; CS _n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I _{DD2P1}	V _{DD1}	
	I _{DD2P2}	V _{DD2}	
	I _{DD2P,in}	V _{DDQ}	

Table 41 — I_{DD} Specification Parameters and Operating Conditions

Notes 1, 2 & 3 apply for all values. CA bus is comprised of RAS_n, CAS_n, WE_n, and A[msb:lsb].

Parameter/Condition	Symbol	Power Supply	Notes
Idle power-down standby current with clock stop: CK = LOW; CKE is LOW; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I_{DD2PS1}	V_{DD1}	
	I_{DD2PS2}	V_{DD2}	
	$I_{DD2PS,in}$	V_{DDQ}	
Idle non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are switching; Data bus inputs are stable	I_{DD2N1}	V_{DD1}	
	I_{DD2N2}	V_{DD2}	
	$I_{DD2N,in}$	V_{DDQ}	
Idle non-power-down standby current with clock stopped: CK = LOW; CKE is HIGH; CS_n is HIGH; All banks are idle; CA bus inputs are stable; Data bus inputs are stable	I_{DD2NS1}	V_{DD1}	
	I_{DD2NS2}	V_{DD2}	
	$I_{DD2NS,in}$	V_{DDQ}	
Active power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I_{DD3P1}	V_{DD1}	
	I_{DD3P2}	V_{DD2}	
	$I_{DD3P,in}$	V_{DDQ}	
Active power-down standby current with clock stop: CK = LOW; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I_{DD3PS1}	V_{DD1}	
	I_{DD3PS2}	V_{DD2}	
	$I_{DD3PS,in}$	V_{DDQ}	
Active non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I_{DD3N1}	V_{DD1}	
	I_{DD3N2}	V_{DD2}	
	$I_{DD3N,in}$	V_{DDQ}	

Table 41 — I_{DD} Specification Parameters and Operating Conditions

Notes 1, 2 & 3 apply for all values. CA bus is comprised of RAS_n, CAS_n, WE_n, and A[msb:lsb].

Parameter/Condition	Symbol	Power Supply	Notes
Active non-power-down standby current with clock stopped: CK = LOW; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I_{DD3NS1}	V_{DD1}	
	I_{DD3NS2}	V_{DD2}	
	$I_{DD3NS,in}$	V_{DDQ}	
Operating burst READ current: $t_{CK} = t_{CKmin}$; All banks active; BL = 4; RL = 3; CA bus inputs are switching; 50% data change each burst transfer	I_{DD4R1}	V_{DD1}	5
	I_{DD4R2}	V_{DD2}	
	$I_{DD4R,in}$	V_{DDQ}	
Operating burst WRITE current: $t_{CK} = t_{CKmin}$; All banks active; BL = 4; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer	I_{DD4W1}	V_{DD1}	
	I_{DD4W2}	V_{DD2}	
	$I_{DD4W,in}$	V_{DDQ}	
All-bank REFRESH burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCmin}$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	I_{DD5IN}	V_{DDQ}	
All-bank REFRESH average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable	I_{DD5A1}	V_{DD1}	
	I_{DD5A2}	V_{DD2}	
	$I_{DD5A,in}$	V_{DDQ}	
Self refresh current (Standard Temperature Range): CK = LOW; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable Maximum 1x self refresh rate	I_{DD61}	V_{DD1}	4, 6
	I_{DD62}	V_{DD2}	
	I_{DD6IN}	V_{DDQ}	

Table 41 — I_{DD} Specification Parameters and Operating Conditions

Notes 1, 2 & 3 apply for all values. CA bus is comprised of RAS_n, CAS_n, WE_n, and A[msb:lsb].

Parameter/Condition	Symbol	Power Supply	Notes
Self refresh current (Elevated Temperature Range): CK = LOW; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I_{DD6ET1}	V_{DD1}	7, 6
	I_{DD6ET2}	V_{DD2}	
	$I_{DD6ET,in}$	V_{DDQ}	
Deep power-down current: CK = LOW; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable	I_{DD81}	V_{DD1}	7
	I_{DD82}	V_{DD2}	
	I_{DD8IN}	V_{DDQ}	

NOTE 1 Published I_{DD} values are the maximum of the distribution of the arithmetic mean.

NOTE 2 I_{DD} current specifications are tested after the device is properly initialized.

NOTE 3 All other channels are in idle power-down standby with clock-stopped state (I_{DD2PS})

NOTE 4 The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the elevated temperature range.

NOTE 5 Guaranteed by design with output reference load and minimum 1 V/ns slew rate.

NOTE 6 This is the general definition that applies to full-array SELF REFRESH.

I_{DD6ET} and I_{DD8} are typical values, are sampled only, and are not tested.

11 Electrical Characteristics and AC Timing

11.1 AC Timings

Table 42 — AC Timings

	Parameter	Symbol	Wide I/O 200MHz		Wide I/O 266MHz		Unit
	Clock Timing		min	max	min	max	
1	Average Clock Period	tCK(avg)	5	100	3.75	100	ns
2	Average high pulse width	tCH(avg)	0.45	0.55	0.45	0.55	tCK
3	Average low pulse width	tCL(avg)	0.45	0.55	0.45	0.55	tCK
	Read Parameters						
1	DQ output data access time from CK	tAC	1	5	1	5	ns
2	DQS output access time from CK falling edge	tDQSCK	1	5	1	5	ns
3	rank-to-rank DQS delay	tDQSDQS	1.8	2.2	1.8	2.2	tCK
4	Average DQS High Pulse Width (slice)	tDQSH	0.9	1.1	0.9	1.1	tCK
5	Average DQS Low Pulse Width (slice)	tDQSL	0.9	1.1	0.9	1.1	tCK
6	Average DQS Low Pulse Width (stack)	tDQSLC	TBD	TBD	TBD	TBD	tCK
7	DQ output setup time from DQS	tQS	1.0		0.8		ns
8	DQ output hold time from DQS	tQH	1.0		0.8		ns
9	DQS full preamble time	tRPRE	0.9	1.1	0.9	1.1	tCK
10	DQS short preamble time	tRSPRE	0.4	0.6	0.4	0.6	tCK
11	Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK
12	DQS low-Z from clock falling edge	tLZ(DQS)	0.5		0.5		ns
13	DQ low-Z from clock	tLZ(DQ)	0.5		0.5		ns
14	DQS high-Z from clock falling edge	tHZ(DQS)		5		5	ns
15	DQ high-Z from clock	tHZ(DQS)		5		5	ns
	Write Parameters						
1	DQ and DM input setup time	tDS	1		0.8		ns
2	DQ and DM input hold time	tDH	1.25		1		ns
3	DQ and DM input pulse width	tDIPW	0.7		TBD	TBD	tCK
	CKE Input Parameters						
1	CKE min. pulse width (high and low pulse width)	tCKE	3		3		tCK
	Command Address Input Parameters						
1	Address and control input setup time	tIS	1		0.8		ns
2	Address and control input hold time	tIH	1.25		1		ns
3	Address and control input pulse width	tIPW	0.7		TBD	TBD	tCK
	Mode Register Parameters						
1	Mode Register Write command period	tMRW	2		2		tCK
2	Status Register Read command period	tSRR	2		2		tCK
3	Read of SRR to next valid command	tSRC	RL+4		RL+4		tCK
	Wide I/O SDRAM Core Parameters						
1	ACTIVE to ACTIVE command period	tRC	tRAS+tRP		tRAS+tRP		ns

Table 42 — AC Timings

2	CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	max(15, 3tCK)		max(15, 3tCK)		ns
3	Self refresh exit to next valid command delay	tXSR	tRFC+10		tRFC+10		ns
4	Exit power down to next valid command delay	tXP	max(10, 2tCK)		max(10, 2tCK)		ns
5	CAS to CAS delay for Read	tCCD Read	2		2		tCK
6	CAS to CAS delay for Write	tCCD Write	1		1		tCK
7	RAS to CAS Delay	tRCD	18		18		ns
8	Row Precharge Time	tRP	18		18		ns
9	Row Active Time	tRAS	42	70000	42	70000	ns
10	Write Recovery Time	tWR	max(15, 3tCK)		max(15, 3tCK)		ns
11	Internal Write to Read Command Delay	tWTR	max(15, 2tCK)		max(15, 2tCK)		ns
12	Active bank A to Active bank B	tRRD	10		10		ns
13	Two bank active window	tTAW	50		50		ns
14	Minimum Deep Power Down Time	tDPD	500		500		us



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